# CHAPTER 7

# PCB DESIGN FOR HIGH-SPEED CIRCUITS

The previous layout suggestions are relatively general and can be applied to most circuits to reduce electromagnetic compatibility (EMC) problems, almost regardless of the circuit function. In high-speed systems, where there are many signal lines carrying high-speed signals with high rise and fall times (e.g. clock signals, data busses, address busses) attention needs to be paid to the effect of track and termination impedance using transmission line principles.

The correct application of transmission line principles also requires the application of some mathematics. Whereas the previous suggestions may have seemed intuitive and their application not very scientific, they have in fact been derived from some of the following principles and mathematical derivations. The maths has deliberately been left out of the previous suggestions to make their application more accessible. Unfortunately, the following principles rely on more rigorous rules and formulae that cannot be too generalised if they are to work correctly.

## 7.1 Controlled Impedance Tracking

In a high-speed digital system it is not sufficient to simply lay all the fast signal tracks 'first', as most signal lines could be classified as 'fast'. As well as keeping these tracks short they must maintain very close impedance matching to each other and their end termination needs to match the line impedance to reduce signal delay and reflection. What this suggests is that at high-signal speeds (typically in excess of 50 MHz) there is going to need to be as much attention paid to the mechanics of layout detail as is given to the circuit design itself. The techniques for layout are similar to those used by designers of microwave circuits, where physical layout and track dimensions are an integral part of the circuit design process.

It is when dealing with high-speed designs and trying to produce impedance controlled tracking that the need for the mechanical printed circuit board (PCB) design data is required (see Appendix B). The track mechanical dimensions are important as well as PCB layer characteristics, particularly track width ($w$), track thickness ($t$) and track length ($l$). These are defined by the designer at the layout stage, although length is dictated as much by component siting and pin-out as by deliberate track design. Consequently, the PCB designer can exhibit full control over

these parameters and minimise EMC and potential high-speed functionality problems at a very early stage.

Control of the PCB material and properties needs exercising by the manufacturer of the PCB and you may need to use a different supplier for high-speed PCBs than low-speed boards. In particular, the supplier has to be able to offer controlled impedance boards to ensure that all the design effort put into ensuring the PCB design is optimised for EMC performance is not lost due to poor quality control at the PCB supplier.

There are two forms of controlled impedance tracks (transmission lines) possible on a PCB: the microstrip and the stripline. The microstrip is a track on the surface of the PCB running above a ground plane. The stripline is embedded within the PCB and between two ground planes. Although the text refers to the tracks being over a ground plane, the supply plane also provides a coupling reference for tracking, hence the tracks above supply planes or between supply and ground also utilise the transmission line track principles. Each tracking scheme will be dealt with separately as the equations for dealing with them are different. It is possible to mix the two and certainly not uncommon to have both on a PCB. In fact it would be difficult to have an embedded stripline only without surface microstrip tracking, as any surface tracks would share a common ground plane, even if the surface tracks had not been deliberately designed as high frequency tracks.

The characteristic impedance of a track is a measure of the characteristic inductance ($L_o$) and capacitance ($C_o$) per unit length of track;

$$Z_o = \sqrt{\frac{L_o}{C_o}} \qquad 7.1$$

The characteristic impedance is measured in ohms (Ω) and in itself does not vary with track length. It is this impedance that is to be controlled and matched between synchronous signals if correct high-speed designs are to be realised without EMC problems.

Another parameter which is important to high-speed signals and in transmission line application is the speed of the signal (signal velocity, $v_s$). The electrical signal travels at a slower rate than in a bare copper wire due to the influence of the dielectric medium:

$$v_s = \frac{c}{\sqrt{\varepsilon_{eff}}} \qquad 7.2$$

Where $c$ is the speed of the electromagnetic wave in free space ($3 \times 10^{-8}$ m/s) and $\varepsilon_{eff}$ is the effective relative dielectric of the substrate. In a high-speed circuit it is not the actual velocity that is important but the propagation delay this reduced velocity produces. The propagation delay ($\tau_{pd}$) is the reciprocal of the velocity but usually expressed in appropriate dimensional terms such as picoseconds per mm (ps/mm) or nanoseconds per foot (ns/ft). (Note: 10 ps/mm = 3.05 ns/ft)

The propagation delay can also be expressed in terms of the characteristic inductance and capacitance of the track:

$$\tau_{pd} = \sqrt{L_o C_o} \qquad 7.3$$

The characteristic inductance and capacitance could therefore be found for any given track from determining impedance and propagation delay. The characteristic inductance varies with the track width, length and to a small extent track thickness, in general wider tracking reduces the characteristic inductance. The characteristic capacitance also varies with track dimensions and with PCB dielectric and layer thickness, wider tracking increases the characteristic capacitance as does a thinner layer build. Although characteristic inductance is rarely used except for some simulation exercises, the characteristic capacitance is an important parameter to determine the loading on driver circuits, and this can in itself limit the design freedom available with certain impedance controlled circuit boards.

General equations for the characteristic inductance and capacitance can be derived from the above characteristic impedance and propagation delay equations:

$$L_o = Z_o \tau_{pd} \text{ and } C_o = \frac{\tau_{pd}}{Z_o} \qquad 7.4$$

These equations can be used where necessary, but caution should be used with the units especially if using mixed imperial and metric terms. For example a track of 50Ω with a propagation delay of 10 ps/mm, will exhibit 0.5 nH/mm characteristic inductance and 0.2 pF/mm characteristic capacitance. These equations are usually easier to use than rearranging the equations derived directly from the impedance that follow and include track dimensions directly, also any anomalies due to dielectric constant need only be accounted for once in the impedance or propagation delay calculations.

## 7.1.1 Surface Microstrip Tracking

The impedance of a single track over a reference plane is controlled by maintaining a fixed distance to the plane and using constant track width over the length of the track.


**Figure 7.1**
Surface microstrip track

When a single ground plane is used, either on double sided or multilayer PCB, and the tracking is on the surface the characteristic impedance ($Z_o$) is given by:

$$Z_o = \frac{87}{\sqrt{\varepsilon_{eff}} + 1.41} \ln\left(\frac{5.98\,h}{0.8\,w + t}\right) \qquad 7.5$$

Where $h$ is the distance between the track and ground plane (layer thickness), $w$ is the track width, $t$ is the copper thickness and $\varepsilon_{eff}$ is the effective relative dielectric of the substrate.

Some confusion has occurred with the value for effective dielectric constant for microstrip applications. This is due to the fact that the signal field travels partially through air and partially through the laminate dielectric for a surface microstrip track, hence the effective dielectric constant ($\varepsilon_{eff}$) can be calculated from the PCB dielectric constant ($\varepsilon_r$) using the equation:

$$\varepsilon_{eff} = \left(\frac{\varepsilon_r + 1}{2}\right) + \left(\frac{\varepsilon_r - 1}{2}\right)\left(\frac{1}{\sqrt{1 + 10\frac{h}{w}}}\right) \qquad 7.6$$

This can be quite cumbersome and a value for FR4 of $\varepsilon_{eff} = 3.5$ is commonly used for surface microstrip tracking. As a first approximation for other materials a divisor of 1.35 could be used for the commonly quoted relative dielectric value. Note this does not affect the value used for the calculation of line capacitance (i.e. $\varepsilon_r = 4.7$ for FR4) as the effective capacitance is contained solely in the dielectric material and is not fringing the air above the track.

It is quite usual to ignore the track thickness term ($t$) as this is much smaller than the width ($t<<w$) and this simplifies the maths. As an example, consider a 1 mm wide track which is 0.5 mm above the ground plane on an FR4 substrate, the transmission line impedance approximates to 52Ω, hence a similar value of termination would be required to match this on a high-speed digital signal line and the driving circuit should be capable of feeding this value of impedance. This value would also provide a good match for a 50Ω coaxial cable interface track (between driver/receiver circuit and connector).

An additional design constraint with surface microstrip lines is the effect of the solder resist mask. The solder resist adds a layer of dielectric above the tracking and can effectively reduce the impedance by between 1Ω and 3Ω depending on thickness. This effect of solder resist is commonly ignored, but in long lines, low-impedance tracks or matching between different types of track construction its effect may have to be considered.

The speed of the signal is affected by this tracking and will need consideration for matching between circuits such as distributed clocks in a synchronous digital system. The propagation delay ($\tau_{pd}$) of a microstrip track is governed by the dielectric of the substrate via the equation:

$$\tau_{pd} = 3.337\sqrt{0.475\,\varepsilon_r + 0.68\varepsilon_{eff}} \qquad 7.7$$

The equation as written is in units of picoseconds per mm (ps/mm). This equation is commonly used as an empirical approximation for microstrip tracking rather than the standard velocity equation and effective dielectric constant. There are differences in the results when using the above equation and the theoretical standard velocity equation, which are relatively small. The above equation has become a standard textbook formula and is used often without knowledge of the approximations to the

effective dielectric implied ($\varepsilon_{eff} = 0.475\ \varepsilon_r + 0.68$). I believe one of the primary reasons for the use of this approximation is the poor control that is exhibited in the dielectric constant of PCB laminate materials, resulting in simple mathematical approximations of this type becoming *de facto* standards. The above equation will be used here for consistency with other texts; however, the theoretical equation below is believed to be a more accurate formula providing an accurate effective dielectric constant can be determined:

$$\tau_{pd} = 3.337\ \sqrt{\varepsilon_{eff}} \qquad 7.8$$

It is often the delay between tracks that is more important than absolute signal propagation delay, as the delay between a clock and data signal can affect functionality as well as EMC. For example, on standard FR4 the signal delay is 5.69 ps/mm, imagine we had a microprocessor in a 255 pin pinned grid array (PGA) package, where pin 1 is the master clock (MCLK), and pin 21 is the lowest address line (ADDR0), separated by 40 mm across the package. Ignoring any internal delays within the silicon, a device near pin 1 which requires both clock and this address would see a 228 ps signal edge delay when these pins are supposedly synchronously switched. Although relatively minor in itself we are now beginning to broaden the switching edges, even though the frequency remains constant, we are introducing small delays into the switching edges and hence to the power demand.

The delay may seem minor on a single package; however, over say a 300 mm backplane the signal delay is just over 1.7 ns. As clock speeds exceed 50 MHz in a system this delay is close to the rise time and a significant part of the pulse width, functionality as well as EMC may be compromised. Certainly, real-time systems would have trouble synchronising multiple processing boards over such a large backplane at 50 MHz data rates.

## 7.1.2 Embedded Microstrip Tracking

A microstrip track can be embedded in the laminate if the PCB has a build on top of the microstrip tracking layer, for bias tracking for instance or to protect the tracking integrity during circuit manufacture. Although relatively uncommon this arrangement is possible. The above equations still hold, but the characteristic impedance is changed as the effective dielectric constant approaches that of the laminate.

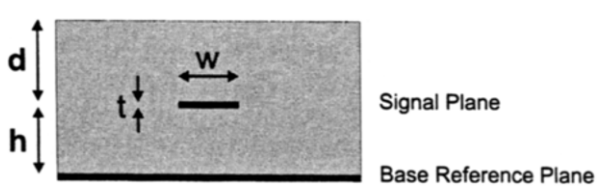



**Figure 7.2**
Embedded microstrip

If the distance between the microstrip and ground plane ($h$) is equal to, or less than, the distance between the microstrip and air ($d$) then the relative dielectric constant of the laminate should be used to calculate the characteristic impedance (i.e. if h ≤ d then $\varepsilon_{eff} = \varepsilon_r$).

For a surface layer build which is in between the track to plane distance ($0<d<h$), the effective dielectric constant can be calculated from the equation:

$$\varepsilon_{eff} = \varepsilon_r[1 - \exp(\frac{-1.55(h + d)}{h})] \qquad 7.9$$

This value can then be substituted into the microstrip impedance equation. If we re-examine our 1 mm wide track 0.5 mm above the ground plane with a prepreg build of 0.25 mm above ($\varepsilon_{eff} = 4.24$), the characteristic impedance is 48Ω, a 4Ω decrease over the surface stripline value. This may seem an insignificant difference and is one of the reasons that many designers use the standard dielectric constant ($\varepsilon_r$) rather than the effective dielectric constant ($\varepsilon_{eff}$), as the differences produced are usually less than 10% of the actual value.

Using the de facto standard equation for propagation delay would indicate that there is no change in signal velocity. This is not true but the changes are relatively small until the dielectric layer above the track is equal to, or greater than, the track to ground separation. At this point the signal velocity should equal that of a stripline as the signal is travelling completely in the PCB dielectric medium.

These equations will be required where there are several layers carrying high-speed signals over a single ground plane. Impedance matching between signals on different layers can be achieved by careful design. If a signal is tracked over several layers the mathematics become quite complex as the characteristic impedance changes between layers, and at vias, hence reflections could occur and this could be one situation where changing the track width becomes necessary to impedance match between tracking layers. Maintaining signals tracks between devices within a single layer will always provide the simplest analysis and usually the quietest solution.

## 7.1.3 Stripline Tracking

Embedded tracking between two ground planes (or power planes) which are equally spaced from the tracking layer is considered as balanced stripline tracking. This is the

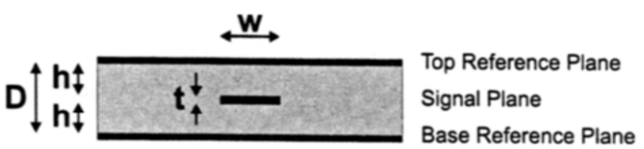



**Figure 7.3**
Embedded stripline track

quietest tracking method for signals as the field is contained totally within the PCB laminate, although some fringing can occur if the track is close to the PCB edge.

With a track embedded between two equidistant ground planes, the track impedance is given by:

$$Z_o = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{1.9D}{0.8\,w + t}\right) \qquad 7.10$$

Where $D$ is the separation of the ground planes ($D = 2h+t$). In using stripline tracks the signal field is contained within the PCB so the standard relative dielectric constant of the laminate can be used (i.e. $\varepsilon_r = 4.7$ for FR4). For example, again consider a 1 mm wide track embedded between two ground planes 1 mm apart (for comparison with the microstrip calculation and assuming $t<<w$). The stripline track characteristic impedance is 24Ω, less than half that of the surface microstrip using a similar build and half of the embedded microstrip construction. Stripline can be equated to parallel embedded microstrips of similar build, hence stripline will offer a lower impedance for a similar build structure than its microstrip equivalent.

The stripline does produce a slightly lower signal velocity than the microstrip, hence an increased signal propagation delay:

$$\tau_{pd} = 3.337\sqrt{\varepsilon_r} \qquad 7.11$$

On standard FR4 the signal delay is 7.23 ps/mm, indicating that microstrip may be better than stripline for the fastest signals with respect to propagation delay. But stripline is the lowest noise tracking scheme from a radiated noise viewpoint as the tracks are fully enclosed on two sides and the impedance is lower.

Considering our previous example of a 255 PGA with 40 mm pin spacing between synchronised signals, the delay is 289 ps between pins at opposite edges of the package. Over a 300 mm backplane the delay is increased to 2.1 ns using stripline compared with the microstrip 1.7 ns. It is physical effects such as this that limit address and data backplane speeds in digital systems to frequencies much lower than the microprocessor clock speed.

The stripline can be further enhanced for signal immunity and radiation by running vias along either side, producing a completed ground shield, the track then approximates to a coaxial cable and the above equations no longer hold. This would produce a further reduction in signal velocity and hence increase in propagation delay. In general, producing coaxial structures within the PCB is not required and adequate noise performance can be achieved by using a suitable transmission line structure and spacing tracks adequately.

### 7.1.4 Dual Stripline Tracking

Striplines can have multiple tracks on separate layers within the stripline structure, or have single tracks which are offset from each of the ground planes. This changes the equations for characteristic impedance, propagation delay remains unchanged as

the effective dielectric constant remains the same. The characteristic impedance becomes:

$$Z_o = \frac{80}{\sqrt{\varepsilon_r}}[1 - \frac{h}{4(h + d + t)}] \ln [\frac{1.9(2h + t)}{0.8\ w + t}] \qquad 7.12$$

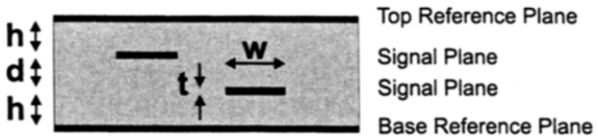



**Figure 7.4**
Dual stripline tracking

The impedance of a dual stripline using 1 mm wide tracks with 0.5 mm layer builds ($h = d = 0.5$ mm) would be 28Ω (assuming $w >> t$ and $h >> t$).

It would be expected that alternate layers within this type of dual stripline build would be tracked orthogonally (i.e. at right angles to each other). This minimises cross-talk by minimising common capacitance between tracks. With tracking layers equally spaced from the ground planes, the impedance for a track is the same on either layer, hence this would be a suitable method for tracking complex wiring arrangements over two tracking layers with matched impedances.

## 7.1.5 Cross-over Capacitance

Cross-talk occurs between signal lines which have mutual inductance or capacitive coupling. Mutual inductance within a PCB is extremely small and most track cross-talk is generated due to mutual capacitance. The major capacitive coupling for PCB tracking occurs at cross-over points, where tracking from different layers cross.

The individual cross-over points each have a very small amount of capacitive coupling; however, there may be tens or hundreds of cross-overs, hence the coupling can become significant.

The track-to-track capacitance can be estimated using the equation:

$$C_c = \varepsilon_o \varepsilon_r \frac{(w_1 + 0.8h)\ (w_2 + 0.8h)}{h} \qquad 7.13$$

This differs from the standard parallel plate equation due to the influence of the track close to the actual cross-over creating a slightly modified area value. The equation depends on the distance between the tracks ($h$) being small and providing the track widths ($w_1$ and $w_2$) are at least twice the separation ($w_1 \geq 0.5h$, $w_2 \geq 0.5h$). When

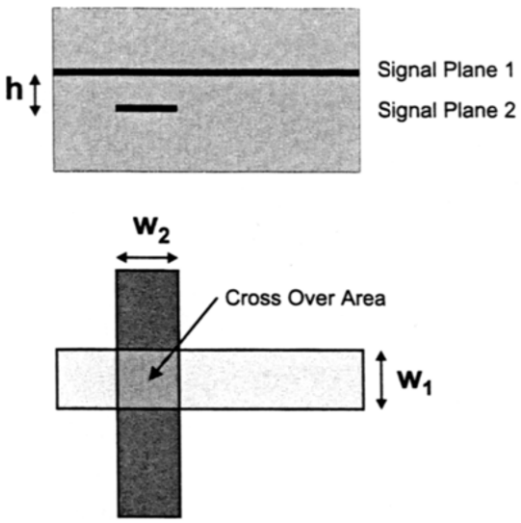



**Figure 7.5**
Cross-over tracking

using fine tracks or large separations the standard parallel plate equation will suffice as a first approximation.

On standard FR4 with two 1 mm tracks separated by 0.5 mm the single cross-over capacitance is 0.16 pF ($\varepsilon_o$ = 8.854 pF/m, $\varepsilon_r$ = 4.7). This magnitude of separation is relatively large and generally the separation on a dense PCB will be in the region of 0.2 mm, increasing the coupling capacitance to 0.4 pF per cross-over. Although the value per cross-over is small it can rapidly sum for dense PCBs to several pico-Farads of capacitance which will not only slow signals but will couple many signal lines together.

## 7.1.6 Termination and Line Length

A transmission line with a characteristic impedance ($Z_o$) will require resistive termination that matches this line impedance, which allows transmission of wideband signals without degradation. If the trace is unterminated reflections and ringing can occur due to the impedance mismatch. These noise problems due to impedance mismatch can create false triggering and offset switching levels, hence reduce noise margin and create emissions.

Not all lines necessarily require termination; there is a critical length ($l_{max}$) at which the tracking becomes 'electrically long'. The on-set of an electrically long track occurs when the propagation delay of the tracking ($\tau_{pd}$) becomes a significant part of the signal rise time ($\tau_r$), defined by the Nyquist criteria:

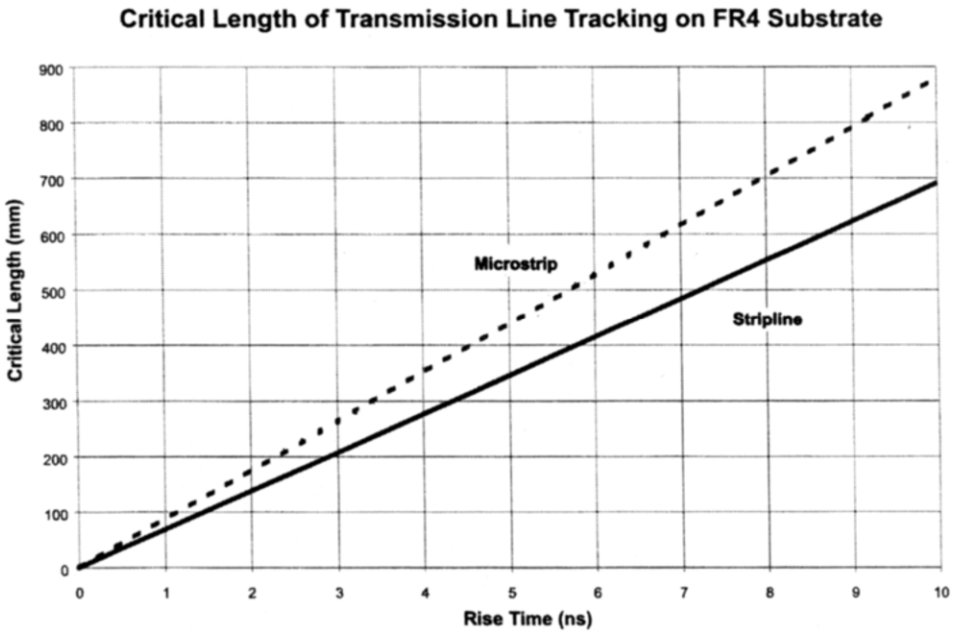



**Figure 7.6**
Critical length for FR4

$$l_{max} = \frac{\tau_r}{2\tau_{pd}} \qquad 7.14$$

With knowledge of the rise time and tracking structure (microstrip or stripline) this critical track length can be determined. For example, assuming ALS logic is used with a maximum rise time quoted as 4 ns, using microstrip tracking on FR4 the maximum unterminated line length is 351 and 277 mm for a stripline track. These seem very long and except for backplane design it could be inferred from these results that most tracking will not be electrically long, but problems could be encountered as the specification for rise time is the maximum value. In reality the ALS logic drivers could easily be exhibiting typical rise times of 0.5 ns, which would see microstrip lines of 44 mm or stripline tracks of 35 mm as electrically long. With modern integrated circuit (IC) packages these distances can occur across the package, let alone between different devices.

As IC manufacturers reduce the dimensions of their transistors, the rise times of their devices will inevitably fall, hence in PCB design termination is going to become necessary to maintain upgradability. Last year's ALS logic device may have twice the rise time of this year's, but the specification will remain the same so there will be no way of knowing what minimum rise time the device will exhibit.

## 7.1.7 Device Loading

So far the discussion has concentrated on the effects of the tracking line only; however, the true line impedance and propagation delay will also be affected by the loading of devices on the line. Even unconnected device pins and sockets add up to 4 pF of capacitance and vias and plated through holes can add up to 0.8 pF of capacitance and up to 4 nH of inductance per feature. Consequently, the true transmission line impedance should include these effects.

It is the capacitive loading ($C_D$) of the devices and track features that produce the loaded impedance ($Z_{LO}$) and propagation delay ($\tau_{Lpd}$) of a track.

$$Z_{LO} = \frac{Z_o}{\sqrt{1 + \frac{C_D}{C_O}}} \qquad 7.15$$

$$\tau_{Lpd} = \tau_{pd}\sqrt{1 + \frac{C_D}{C_O}} \qquad 7.16$$

It is this loaded propagation delay ($\tau_{Lpd}$) that should be used to determine if a track is a transmission line (i.e. electrically long). This will of course further reduce the effective line length prior to the onset of transmission line effects and slow signal velocity within a system. Consequently, for accurate matching of signal delays and impedance, not only does the track have to be properly designed, but device loading should be matched. Device load matching is usually accounted for by the fact that critical signals generally are between the same devices (e.g. between memory and processors, between interfaces and buffer circuitry), only the clock signals may experience significant loading differences.

As an example consider a clock line driving ten 5 pF gates over a 10 cm balanced 50Ω stripline. The characteristic line capacitance is 14.46 pF, hence the loaded impedance is 23.7Ω and the loaded propagation delay is 15.3 ps/mm, half the impedance and twice the delay of the unloaded line. This is part of the reason high-speed clocks have such stringent fan-out rules and why buffering the clock is carried out both on-chip and between devices.

If possible it would also be recommended that loads are evenly distributed along a transmission line. This can be difficult to achieve as the location of devices which load the line are not defined at the initial stages of layout due to their loading effect but their interaction. Hence by the time an assessment of the loading is made the line length and device positions are often already fixed.

## 7.1.8 Reflection and Ringing

The main purpose of using transmission line principles for the design of high-speed signal PCB tracks is to enable signals to be transmitted with the minimum amount of noise and interference. The main source of the interference will come from the signal itself, interacting with the line and loading to create ringing and reflection artefacts

in the PCB trace. These can be minimised if we know the line and loading impedance ($Z_{LO}$) and the impedance of the driver source ($Z_S$) and receiver circuit ($Z_R$).

Reflections are initially caused by mismatch between the impedance of the receiving circuit and the line, the coefficient of reflection at the load ($\rho_R$) is given by the ratio of the impedance mismatch.

$$\rho_R = \frac{Z_S - Z_{LO}}{Z_S + Z_{LO}} \qquad 7.17$$

The mismatch in load and drive source impedance also causes a reflection, again the source reflection coefficient ($\rho_S$) being the ratio of impedance mismatch.

$$\rho_s = \frac{Z_S - Z_{LO}}{Z_S + Z_{LO}} \qquad 7.18$$

The receiver impedance is often high in many logic devices, hence the receiver reflection coefficient is almost 1 ($\rho_R \sim 1$), this produces a full reflection of the drive voltage back to the driver. Consequently, it is most often the driver to loaded line impedance that is the critical parameter determining ringing and reflections in a transmission line track.

If the driver source impedance is less than the loaded line impedance ($Z_S > Z_{LO}$) then reflections at either end of the line occur and a ringing waveform is seen in the line (the signal is 'bounced' from driver to receiver many times, diminishing in magnitude after each reflection). If the source impedance is less than the loaded line impedance ($Z_S < Z_{LO}$) then the driver experiences difficulty in driving the signal into the track and a staircase or stair-stepping voltage is observed on the line.

The ideal is to have matched driver and receiver impedances; however, this is often difficult, particularly with many devices coupled to the line (e.g. microprocessors,

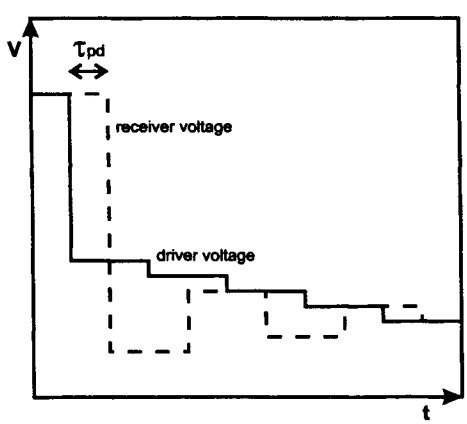



**Figure 7.7**
Staircase stepping voltage due to impedance mismatch

memory and interface on an address bus). It is due to the multiple number of devices that can receive simultaneously that many of the receiver circuits have such a high impedance. Driver impedances are sometimes given, so these may not be as difficult to determine; however, often the high-to-low and low-to-high transitions may offer difference impedances, hence matching of the driver may in fact not be possible. If impedances are unknown but suspected to be significantly higher at the receiver than the source/drive, termination of the transmission line will be necessary to reduce noise problems and ensure signal integrity.

## 7.1.9 Line Termination

To minimise reflection and ringing transmission lines may need to be terminated using additional components. The type of termination will depend on the line impedance and the drivers and receivers connected along the line.

Circuits which are driving into a line from a single driver with multiple receivers (such as clock circuits) usually have a lower driver source impedance than the line or load impedance. To match the source to either line or load, a series resistor is placed in line with the drive (Figure 7.8a). The value of resistor is usually quite low (typically 10Ω) and usually matches the driver impedance to the line characteristic impedance.

$$R_t = Z_{LO} - Z_S \qquad 7.19$$

The resistor is usually placed immediately after the driver output, between the driving circuit and the transmission line. The inclusion of a resistor in series can cause additional signal delays, especially into capacitively loaded receivers, although with most digital circuits having the clock delayed slightly compared with the data can have beneficial results for system integrity.

The pull down resistor (shunt resistor or parallel termination, Figure 7.8b) is a common technique and is easy to implement. Only one resistor per line is required not one per receiver, unless each resistor is a high value so that the total parallel resistance is equal to the characteristic line resistance. Multiple resistors per receiver circuit is a method which creates an even distribution of terminating impedance, but usually the higher component count is a problem and a single resistor per transmission line is most frequently used. The shunt resistor does not create additional propagation delays but does increase the line drive requirement as the termination impedance is reduced. The line driving circuits must be capable of driving the termination impedance as well as the line impedance, which should be matched ($R_t = Z_{LO}$).

Where the increased DC current drive is unacceptable or undesired the termination can be AC coupled by the addition of a single capacitor per line (Figure 7.7c). The capacitor has to have a low value and high operating frequency (typically 100 pF MLCC type) so that at the transition the impedance of the capacitor is low (near zero) and hence the termination impedance is equal to the resistor alone. The DC impedance after transition reverts to the terminating impedance of the receiver

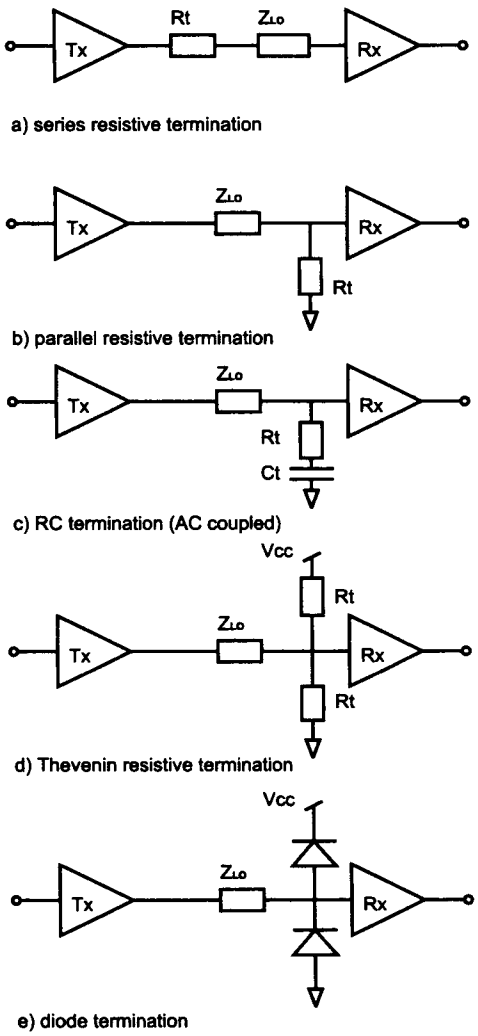
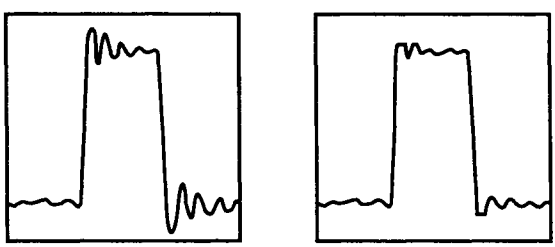



**Figure 7.8**
Termination schemes

circuits, which is usually high, hence there is little DC current flow after transition. This technique reduces the line overshoot and ringing without significantly affecting the steady-state current requirement of the complete circuit. Again the terminating resistor is chosen to match the characteristic line impedance ($R_t = Z_{LO}$). The additional termination capacitance will add to the loading capacitance of the circuit, slowing the signal and reducing the loaded line impedance.

Circuits which feature different impedance for driving high-to-low and low-to-high transitions can be terminated by a Thevenin termination with both pull-up and pull-down resistors (Figure 7.8d). For example, VME bus systems usually feature a 470Ω pull-down and a 330Ω pull-up resistor. This increases current consumption as whether the line is driven high or low, there will be a current flow through one of the resistors. There is also a DC offset on the line of approximately half the supply rail which may reduce the susceptibility of the circuit if the line is in a non-active drive state.

Overshoot and undershoot can be significantly reduced by use of diode termination (Figure 7.8e), this clips both positive and negative transitions to within a single diode drop (typically 0.6 V) without the increased DC power consumption of the Thevenin termination. The diodes have to be selected to be fast enough to operate at the transition rates of the signals and with sufficiently low capacitance to have negligible effect on the line loading. Diode packs featuring multiple line termination pairs are available to simplify placement of this type of termination on bus lines. Strictly speaking diodes do not terminate the line as they are not matching any impedances; however, they may be an adequate solution if the main EMC or signal integrity problem is overshoot or undershoot (or reflections due to these effects), they also provide electrostatic discharge (ESD) protection of the lines.



a) unterminated overshoot, undershoot and ringing

b) diode clipping to reduce overshoot and undershoot

**Figure 7.9**

Diode termination reduces overshoot and ringing

The above termination principles should be applied to differential lines as well as the single-ended transmission schemes shown in Figure 7.8. Differential lines may be individually terminated or cross-linked by resistive or diode schemes.

## 7.1.10 Which Transmission Line?

Microstrip tracking is more popular than stripline due to its lower cost and greater simplicity. There is also additional test and production benefits in having the tracks accessible at the surface of the PCB that makes microstrip more attractive to many

users, but surface tracking also increases the potential for radiated emissions. Microstrip is faster than stripline, however, as noted above for similar dimensions of track microstrip exhibits higher impedance than stripline and is consequently more susceptible to electromagnetic interference.

The stripline method requires at least one additional ground plane, probably several in complex microprocessor designs. The enclosed track construction ensures that both emissions and susceptibility are minimised, particularly useful for long runs such as address bus backplanes. The lower impedance is another beneficial parameter when creating long tracks, but impedance matching to low value lines can increase power consumption (i.e. it takes more power to drive 24 Ω lines than 48 Ω lines at the same data rate).

There are no straightforward rules; it would be recommended that clock lines were distributed via stripline tracking as these are usually the greatest potential noise source in a digital system. Also, having the clock travelling at a slightly slower rate than the signals can help with ensuring that the signal lines have stabilised before the clock signal latches the gates. Having a clock distributed to many circuits can also help in creating the low termination impedance due to the parallel effects of many higher impedance terminations; however, fan-out rules must still be obeyed, regardless of PCB tracking method.

Shorter tracks between local ICs can use microstrip tracking in most cases. It is unlikely that all tracks will be able to be adequately matched for signal delays as many of the larger IC packages can exceed 50 mm between pins on a single device (e.g. 255 pin PGA). Using straight through embedded microstrip tracks could create a time delay between signal edges of over 120 ps on large IC packages. If the system clock frequency exceeds 100 MHz this signal delay approaches 2.5% of the pulse width and begins to become a potential signal integrity problem. As IC manufacturers increase the functionality of silicon devices and pack in more transistors per square millimetre, the size of the packaging seen on PCBs is likely to increase. The majority of these larger devices have all the address lines close together and all the data lines close together, so common sense is being used in the IC design and packaging.

Using serpentine tracks to match the delay for some of the signal tracks is not a common technique but can be implemented when absolute matching of delays is required. Mixing surface and embedded microstrip tracking with stripline is an alternative technique to match the delays between high-density signal tracks across a large IC device package or to a backplane or connector.

## 7.2 Multilayer Build

The construction of layers within a PCB can help with the EMC performance. In particular, with controlled impedance boards it may be necessary to add additional ground and power planes, and the location of these can be chosen to help reduce emissions and susceptibility.

This at first sounds like a recipe for more layers equals better EMC performance. While this may be generally a truism, it has to be tempered with some design input as simply increasing the layer stack in a PCB alone is not the solution. One problem that can occur and should be considered is the overall PCB thickness. The closer the tracking the greater the potential for cross-talk between signals, the lower the impedance and higher the drive (power) requirement, hence greater immunity but with a higher potential for conducted noise and higher manufacturing cost.

## 7.2.1 Number of Layers

The number of layers is almost impossible to calculate with any accuracy or certainty. The previous chapter suggested one tracking layer per five ICs, which is a very loose approximation for simple designs. For high-speed systems the tracking density would be expected to be increased, but the number of layers would not be of this order of magnitude, otherwise most digital systems would have over 20 layers within their PCB.

For high density digital systems an approximation can be obtained from the number of address bits ($A_n$) and the processor speed ($f_{CLK}$ in MHz). Higher bit counts and the faster clock speeds requiring more layers for noise suppression and signal integrity. Again the results are based on empirical observations rather than any mathematical derivations, but a general estimate for the number of layers ($N_L$) can be obtained using:

$$N_L = 5 \log[A_n f_{CLK}] \qquad 7.20$$

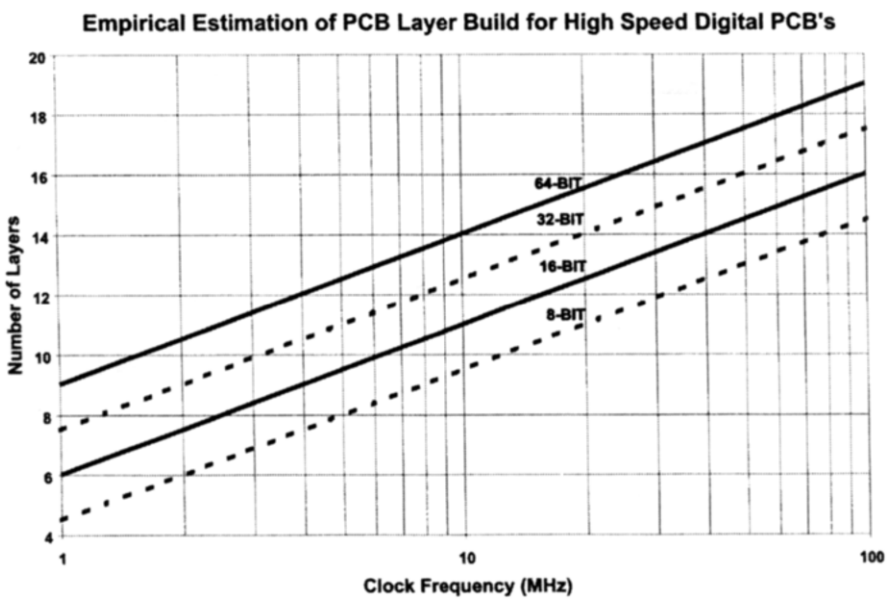



**Figure 7.10**
Number of layers in high-speed digital system PCB designs

This empirical equation should be used as a first approximation only and as an initial gauge of PCB cost. The number of layers suggested is usually slightly pessimistic and fewer layers should be possible.

The applicability of the equation can be examined by using it to estimate the number of layers in PCBs, which you already have worked on. Often the increased layer count suggested may not seem necessary, for example a 16-bit microprocessor system operating at 4 or 66 MHz will not really require any difference in tracking layers for functional performance, but the equation would suggest nine layers at 4 MHz and 12 layers at 66 MHz. These additional layers would be expected to be used to improve the EMC performance (i.e. additional ground planes) and to match the impedance of the faster signal tracking in the 66 MHz system (e.g. matched striplines).

## 7.2.2 Layer Build

The structures of layer build should be similar to the suggestions given for general PCB design, with possibly the inclusion of more ground and power planes and

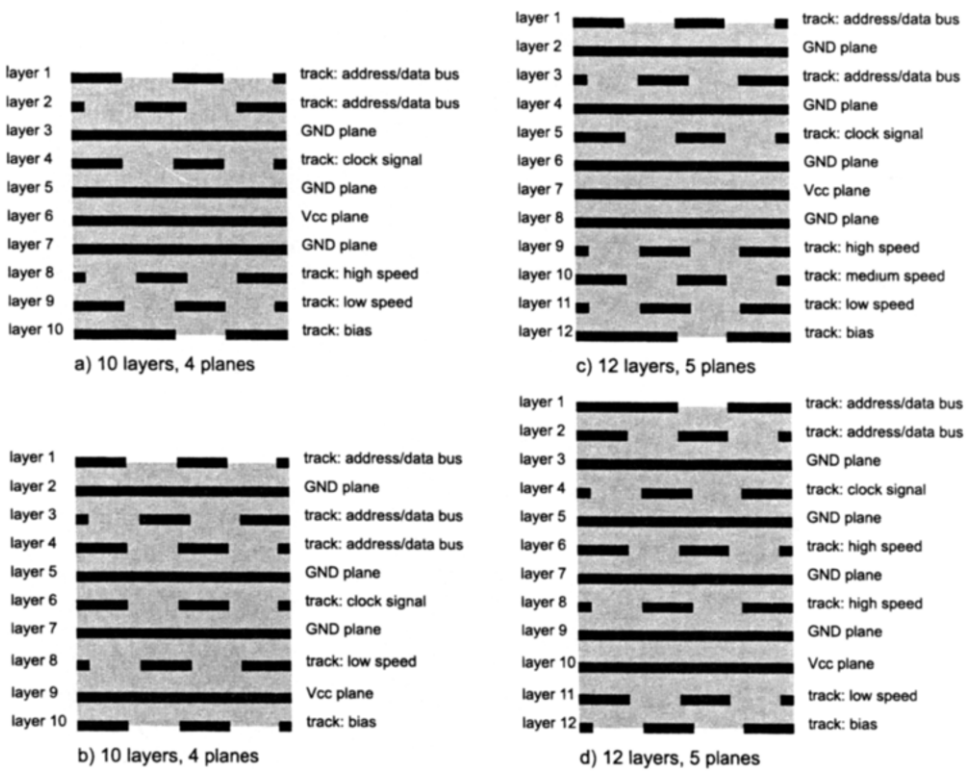



**Figure 7.11**
Example PCB stacks

tighter control over layer thicknesses. With more layers likely in higher-speed designs, it should be possible to dedicate specific layers to specific routeing and tracking functions (e.g. layer 1 for bias tracks, layer 3 for data buses, layer 5 for clock and timing tracks, etc.).

The use of foil build (i.e. prepreg layers between tracking) may be more frequently used in high-speed PCB designs, particularly between ground and power planes. The use of foil build on power planes produces a good high frequency distributed capacitor which improves decoupling with almost no cost implications. Foil build between tracks and ground is generally not recommended as this creates such a low impedance that the signal can be difficult to drive.

As there are going to be several layers of high-speed signals within the PCB there should be multiple ground planes within the structure. A target of one ground plane per two signals layers carrying frequencies above 50 MHz should be aimed for. This allows multiple offset stripline constructions to be arranged as well as surface and embedded stripline tracks. Biasing and lower speed signals can either be tracked on the surface or between a power and ground plane. At clock rates above 100 MHz more stringent transmission line tracking may be required and a ground plane per high-speed tracking layer may be required.

### 7.2.3 Line Spacing

Coupling between high-speed tracks running in parallel can become problematic if the signals are not deliberately paired (e.g. differential signal pairs). Although this effect is small compared with cross-over capacitance the coupling can be further reduced by observing a simple line spacing rule based on the track width ($w$).

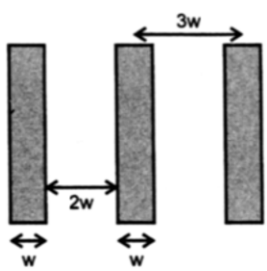



**Figure 7.12**
3w rule for track separation

The rule is sometimes referred to as the $3w$ rule as it suggests that track centres should be at least three times their width apart. This can also be applied to guard rings where the purpose of the ring is solely for radiated noise protection and

deliberate coupling is not intended. The fringing field has fallen to 96% of its value immediately next to the track at this $3w$ distance.

Of course, where tracks are deliberately coupled, the converse would be true and tracks should be close. As a sensible limit a distance between centres of twice the track width provides adequate coupling between signals without risking short circuit problems. Again this can be applied to guard rings where some level of coupling to the guard rail and signal is desired.

## 7.3 Summary

At a seminar on portable systems design a US presenter made a comment about the enquiries they had on their technical helpline, '90% of all the reported problems were caused by noise, 80% of these were solved by layout changes'. I think a similar statement could probably be made about EMC problems within design, although I would doubt the statistics would be quite so high. What this statement does illustrate is the effect that PCB layout can have on a system's performance, both functional as well as for EMC compliance. Any design incorporating a PCB will not cost any more due to following the guidelines given here, but may cost a lot more if they are ignored.