CHAPTER 6

PRINTED CIRCUIT BOARDS

Design and layout of a printed circuit board (PCB) for electromagnetic compatibility (EMC) considerations is probably the most cost-effective measure it is possible to take in the quest for EMC compliance. It is the most cost-effective as it requires no additional components, just the knowledge and experience of EMC layout methods and time spent in applying them. It may also lead to the reduction in filtering requirements, including the number of filters, hence the application of correct PCB layout for EMC could even reduce the cost of compliance. Critical errors in layout causing an EMC problem may not be resolved by the application of additional filters, therefore relaying the PCB may be the only solution and getting it right first time will always offer the lowest cost approach.

There is no single rule for minimising EMC at the PCB level, it requires the application of many design constraints, most of which are general good design practices. As with most other EMC design rules, the basic principle is to minimise bandwidth, reduce cross-talk and produce quiet signals and systems.

It is probable that not all the ideas postulated here can be applied simultaneously to a given circuit, it is up to the designer or layout engineer to decide which are most applicable. As experience is gained it will become less time consuming and more a matter of course for designers; however, at the moment it appears as an extra design burden. It is not the intention of EMC regulations to prevent certain circuits from ever being produced, it just feels that way. It is worth noting that if a 64-bit 166 MHz computer board can be produced that is EMC compliant, most other circuits should be easier.

6.1 PCB Terminology

It is worth considering the terminology for each possible layer within a PCB so that when reading further on we are all 'singing from the same hymn sheet'. When through hole was the dominant component packaging method life was simpler as there were two easily identified layers; the component layer on which the parts were sited and the tracking layer on the opposite side which contained the interconnect. With surface mount not only does the component side contain the interconnect, but both external surfaces can have components placed on them for maximum packing density.

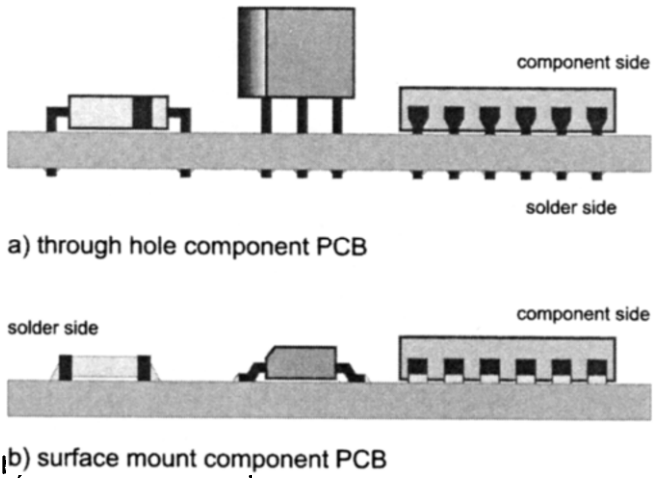

Figure 6.1
Mounting options for PCBs

Component side: any external surface which has the component body sited. For through hole components this is the opposite side to the soldered side. With surface mount both external surfaces could be component sides. The double component sided surface mount PCB is popular in mobile equipment but in most other applications it is still more common to place components on one side only. The component side for surface mount is also the solder side.

Solder side: the side of the PCB to which solder is applied. As noted above this is opposite to the component side for through hole parts and the same as the component side for surface mount.

Buried layer: on a multiple layer PCB, any layer contained within the PCB only (i.e. not on the surface) is called a buried layer.

Tracking layer: this is any layer which contains interconnecting tracks. Tracking can be on the component side, solder side or within the structure of the PCB on boards containing multiple layers. On most PCB designs which contain more than one layer the majority of these layers are tracking.

Plated through holes: vertically interconnecting holes which go between outer surfaces and are metallised (plated) through the hole. These holes are used for through hole components and where the interconnect tracking is on both external surfaces. Plated through holes give very good mechanical attachment to through hole components and are still in common use with connectors and sockets even on boards which otherwise feature all surface mount parts.

Vias: these are interconnections between layers. Vias that go from surface to surface can appear like plated through holes. The function of a via is interconnection not

component attachment, hence often vias are much smaller than plated through holes. Vias can also be buried (sometimes known as blind vias), where the via interconnects two tracks one or both of which are buried within the PCB structure.

Ground plane: a continuous plane of copper within a PCB connected to the circuit ground. It is unlikely that the plane can be completely continuous as usually there are through connections such as plated through holes and vias which create small discontinuities within the plane. On some surface mount designs with a simple interconnect pattern it is possible to create a completely contiguous plane on the PCB. The ground plane is usually contained within the PCB and is not placed on a surface side.

Power plane: as above for ground plane, only these planes carry the supply rails for the circuit. It is worth remembering that circuits can require multiple supply rails for their correct operation, hence multiple power planes or a split single plane may be required for functionality.

Laminate: this is the insulating material, usually of a fibreglass resin compound, that the tracking layer is placed on and separates individual tracking layers from each other. It is the laminate that gives the PCB interconnects a different electrical transmission characteristic than standard insulated wires. Laminate layers are also the rigid layers within a PCB that provide the mechanical strength of the finished board.

Prepreg: these are also insulating layers. Prepreg is an abbreviation for pre-impregnated and is sometimes referred to as 'filler'. The prepreg is thinner than the laminate and is a glass cloth filled with epoxy resin. The prepreg is intended to form a layer on top of buried tracking to produce a flat surface on which to add the next laminate layer and bond the laminates together. Prepreg usually has similar electrical properties to the laminate but is a softer compound. Tracking can be made on to prepreg, this type of construction is known as a foil build.

Moat: this is an area which has no tracking or plane through it. A vertical cross-section of a moat area should consist solely of laminate and prepreg layers.

Hopefully none of the above is new to the reader. The main confusion that occurs is the difference between vias and plated through holes. On surface mount boards there may be no through holes and no direct interconnect between outer surfaces, except via buried layers. With through hole boards the component holes make perfectly reasonable via interconnects and save adding to the board complexity with additional vias. Some PCB manufacturers do not always discriminate between vias and component plated through holes, preferring to call them all plated through holes.

6.2 Construction of a PCB

The level of PCB complexity available to the designer will to some extent determine the amount of good EMC design practices that they can put into effect. As an example, if the product cost allows only a single-sided PCB to be used, then ground

and power planes are immediately excluded from consideration. Even with a single-sided PCB there are still some good and bad design practices that can influence the EMC of the finished circuit.

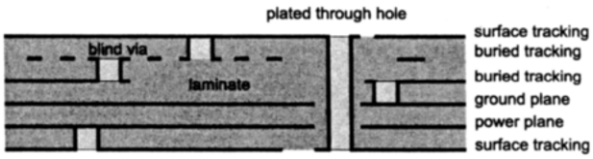

Figure 6.2
6 Layer PCB cross-section

A PCB is constructed from a series of laminate, tracking and prepreg layers in a vertical stack. Within the stack is often a series of drilled holes, plated forming vias between tracking or plated through holes between surfaces. The way these layers are stacked is dependent on the number of layers available for the design. The most popular layer structures are two, four and six layers. The actual number is almost unlimited but the highest in common use is 12 layers. Single-sided (i.e. one layer) boards do appear in very low-cost applications; however, in the majority of modern circuits the limited interconnect possibilities of a single layer are too restrictive.

The process of PCB manufacture has tended to dictate existing common practices for PCB stack structure. The usual advice is to use a balanced stack, that is symmetrical with respect to laminate and prepreg spacings. Symmetrical structure from the inner centre out is also a common theme using equal thicknesses of laminate and prepreg with an even number of tracking layers and ground and supply planes.

There are economical reasons for the use of even layers. The cost of three and four layers is almost equal, the benefit of an additional layer can be costed against a possible increase in packing density (i.e. reduced total board size), hence reduced cost per PCB in volume. In a stack, as the laminate can be metallised on both sides, it is a waste of a laminate layer not to put a pattern or plane on to both sides, hence the PCB stack is going to consist of an even number of metallised layers.

The structure of these layers can be dictated by the user, but there are common themes which are worth considering. The surface layers are almost always tracking layers and rarely contain a plane, this makes sense from a circuit manufacturing viewpoint as it can be impossible to test or debug buried tracking. In four-layer boards the outer layers are the tracking and the inner layers often the power and ground planes. Where a third layer is required for interconnect on a four-layer board the power is sometimes given a routeing pattern within the buried layer and signal tracking added to this layer, but the ground plane is retained. Where power planes are present it is common to have these adjacent to a ground plane and to have

tracking on the outside of these, tracking is rarely placed between ground and supply planes.

Multiple ground planes in high layer stack boards are common, but multiple power planes are not used frequently unless required for functionally (e.g. multiple supply rails such as 5 V and 12 V or ±15 V). Where there is more than one power plane, the planes should be separated from each other by a ground plane or on the same plane and be non-overlapping.

6.3 PCB Design Parameters

The design parameters considered important for the EMC aspects of a PCB design are mainly concerned with the mechanical dimensions of the tracking and layers as well as the dielectric properties of the laminate. The values given in Appendix B are standard for a large number of PCB suppliers but you should consult your own supplier to get the most accurate data. Although the absolute parameters used are going to depend on the individual design there are a few considerations that can be applied across all designs.

Cross-talk between tracks can be reduced by increasing the separation between tracking as this is dominated by capacitive coupling. Track impedance can be controlled by tracking above a ground plane (see section on high speed PCB design). The capacitance between power and ground plane can be maximised by using prepreg between the two (foil build), hence reducing the distance between the 'plates' and forming a distributed capacitor. Try and keep the most sensitive and highest frequency tracks away from any power plane as the power supply line tends to contain a relatively high noise content. Minimise impedance on ground and supply rails by using plane layers when possible, where planes are not available use wide tracking. As individual design considerations are discussed later some of these ideas will be reiterated.

If considering a design using signal speeds in excess of 5 MHz, or using devices with rise times of less than 5 ns, then a multilayer board should be planned from the outset. Although single- and double-sided boards are mentioned in the text below, their use is diminishing rapidly and the cost difference between two and four layers is closing. If in doubt at the start of a design on the complexity to allow for in the PCB stack, a guide can be taken from the number of components to be used and the rule of thumb of one tracking layer per five integrated circuits (ICs) or 20 discrete components. This rule is very general and varies so much by design that its usefulness is questionable, but it is better than nothing and can be used at the concept stage to estimate PCB costs.

Tracks on a PCB add inductance, resistance and capacitance to the circuit. The amount of inductance is relatively constant across substrate types and depends on length of track. The inductance per unit length of copper track is similar to that for a component lead, 1 nH/mm. Resistance of a track depends on the cross-sectional area of the track as well as the length, hence values are usually quoted (when they are

available) in resistance per square for each weight of copper (see Appendix B). The most popular copper weight, 1 oz, gives a typical value of 0.49 mΩ/□.

Capacitance is calculated using the parallel plate equation:

$$C = \varepsilon_o \varepsilon_r \frac{A}{h} \qquad 6.1$$

Where ε_o is the dielectric constant of free space (ε_o = 8.854 pF/m), ε_r is the relative dielectric of the substrate (ε_r = 4.7 for FR4), A is the coverage area and h is the distance between tracks. Therefore a 1 oz copper track, 0.5 mm (0.020") wide, 20 mm (0.8") long over a ground plane on a 0.25 mm (0.010") thick FR4 laminate would exhibit a resistance of 9.8 mΩ, an inductance of 20 nH and a capacitive coupling to ground of 1.66 pF. These values may all seem like low values and even negligible compared with some component parasitics, but there will be many tracks and these will add up to track parasitic elements which equal or exceed several of the component parasitic effects. And, of course, these parasitic effects are under the designers control unlike the component parasitic parameters.

There will, of course, be other design constraints from production or marketing which can restrict some of the options. The restrictions may not be just cost, higher layer stacks create thicker finished boards, some applications such as in handheld equipment and PCMCIA cards may have a severe restriction on board thickness. Similarly, the rigidity of the PCB may be critical for efficient production handling, hence more laminate layers may have to be added to stiffen the product for processing in the manufacture of the finished circuit.

The design constraints for EMC usually come low down on a list of design restrictions but are just as important, if not more so. At the end of the day they can prevent a product reaching the market just as much as the other design constraints. However, few of the other constraints can result in prosecution for failure to comply, which can happen in Europe if a product fails to comply with the EC EMC regulations.

6.4 PCB Layout for EMC

The ideas given are presented in roughly order of effectiveness; therefore, try and apply the first three (segmentation, decoupling and grounding) in some form in all circuit layouts, then as many of the others as is feasible. As mentioned previously, the level of PCB complexity will restrict how many of the layout suggestions given can be implemented.

There may be situations where the only solution to an EMC problem is an increase in PCB complexity to implement more of these design rules. This may prove less expensive than options such as shielding and filtering. It is sometimes difficult to cost out the options when the effectiveness cannot be assessed until the problem is seen and the circuit has been built, or even worse, the end product has failed EMC compliance testing.

6.4.1 Segmentation

Segmentation is also known by the terms quarantining and functional separation. The idea of this principle is to reduce the coupling between circuits by basic physical separation. The actual amount of separation is difficult to specify for all applications and will depend on the wavelength of the signals in each section (one-quarter wavelength gaps being a minimum). As a basic guide, a gap between circuits of approximately 5 mm all around is usually adequate.

Segmentation of circuits is usually performed by using a moated area around each circuit or functional block. Hence there will need to be some patterning of any ground and power planes used. The reason for patterning the ground and supply rails is to prevent a power surge or noise voltage on one circuit block (which may be able to handle the event) being returned via the ground on another circuit block (which cannot tolerate such an event). The ground connections and supply rails will all no doubt meet at the power input to the PCB, but by separating, the loops for supply and ground return are controlled for each circuit.

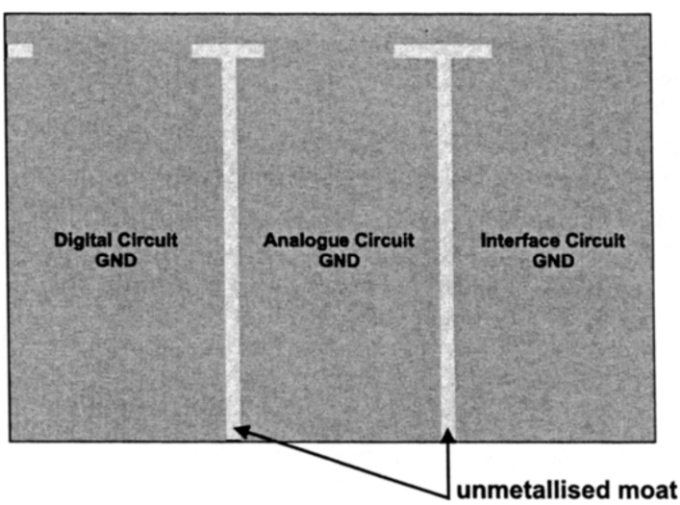

Figure 6.3
Moated ground plane

Segmentation also makes filtering of each circuit block on a PCB simple and reasonably cost effective. For example imagine a PCB has 10 functional blocks using 500 mA each, the total board supply is hence 5 A. A filter for a 5 A DC supply usually contains large inductors, which not only occupy a lot of board area, but are often difficult to place (see section on passive components). Using ten 500 mA filters, the inductors are smaller and each circuit is filtered not only from the power supply unit (PSU) noise, but from each other circuit's noise content. Having segmented circuits

makes this filtering option easier. In reality it is unlikely that all circuits require equal current, hence with individual filters the inductor–capacitor combinations can be optimised for each circuit supply requirement and for an appropriate cut-off frequency, some segments may even be unfiltered. The cost of lower current inductors may not be quite a factor of 10 less than the high current version, but the smaller, lower current rated inductors are definitely lower cost and more suitable to automated PCB assembly methods.

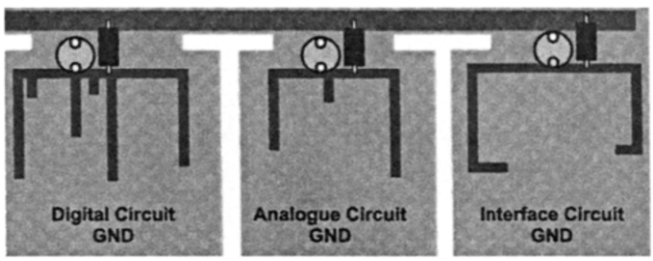

Figure 6.4
Filtered supply rails

Circuits should be segmented by function and/or speed of operation. High speed digital circuits tend to have high instantaneous current demands on clock edges (especially synchronous digital circuits where all the gates switch at the same time, almost). High speed circuits should be placed closer to the PSU inlet than slower circuits such as analogue functions and interface circuits. The placement of high speed circuits close to the PSU reduces the surge demands being observed on the supplies to the other circuit blocks (filtering as mentioned above and adequate

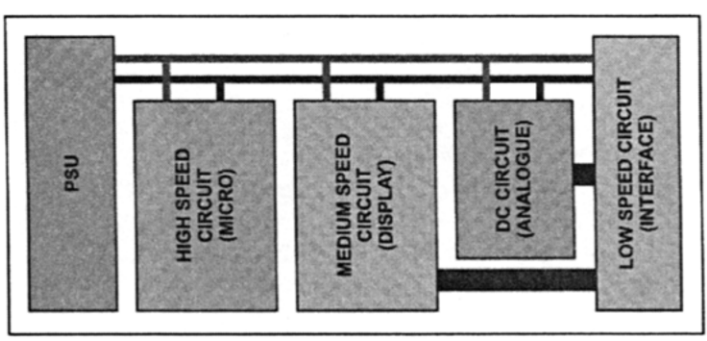

Figure 6.5
Separated function blocks

decoupling also help). It should be borne in mind that it is not the absolute power demand that causes EMC problems within a system, but transients in the power demand.

Circuits which will interface with the outside world or with other PCBs within the end system must be near the PCB edge, there can be no excuse for trailing wires across a PCB within a system. There may be some circuits on a PCB that are known to be noisy, or are intended to handle 'dirty' signals from off-board systems. Filtering may also be required at these circuit inputs, hence within the circuit block a secondary segmentation may be required to handle the off-board signal filters at the PCB interface. A separate moated ground plan for interface circuits would be another good EMC measure, especially if there is a safety ground which could be referenced for ESD and transient suppression circuits directly at the interface socket.

If shielding is ultimately required on certain circuits, by using segmentation at the outset it is easier to shield individual circuit areas rather than the whole PCB. For the purpose of shielding a ground contact will probably need to be available on the PCB surface around the problem circuit. It may therefore be worth bearing this in mind for particularly sensitive circuits and for very high-speed circuits. If not needed the shield can be left off and the only penalty may be a few additional millimetres of gap between circuits, plus the additional ground tracking (see guard ring, covered later in grounding techniques). The provision for shielding of individual circuit segments will not only make the shielding more effective by identifying the critical circuits, but will also minimise the shielding costs as the cost of a shield is primarily governed by the size of the shield required.

6.4.2 Decouple Local Supplies and ICs

The most common way circuits interfere is through their common power supply rails. Maintaining separate decoupling to each circuit area reduces the ability of noise on one circuit's supply rail getting through to another. If space and cost permits filter each supply function on the DC rails as suggested above, a simple LC filter is usually adequate. This filter can remove the need for some mains filtering as it stops noise getting back to the mains supply, as well as reducing cross-talk between circuits. Not forgetting also that DC capacitors and inductors are much smaller and cheaper than their mains counterparts.

Each individual PCB should have a large bypass capacitor (referred to as bulk or reservoir capacitor) at the supply input to the PCB. Bypass and decoupling capacitors are usually not of the same value or construction (see section on capacitors). It would be expected that the bypass capacitor is typically between 10 and 100 μF per PCB and often either an aluminium electrolytic or tantalum type. The bypass capacitor acts as a low frequency ripple filter and potential reserve supply for sudden board demands (e.g. switching operations). The capacitance reservoir reduces localised power demands causing the main supply line to 'dip' by providing current surges locally. The bypass capacitor should be located at the point at which the power enters the PCB, either at the socket or wire terminals connecting the PCB to the system PSU.

Each and every individual IC should have a decoupling capacitor of a few nF, usually of ceramic construction. Decoupling capacitors provide a high frequency, low impedance route to ground for IC switching noise as well as a small reserve for transient power demands. Ceramic is a high frequency dielectric and is the best material for this application (see section on decoupling capacitors for most suitable values).

The decoupling capacitors should always be located close to the IC and closest to the supply pin (usually the Vcc pin). This reduces the tracking impedance to the capacitor, hence maintains the effectiveness of the decoupling capacitor at high frequencies and with fast edge rates. Often the effectiveness of using a decoupling capacitor is lost due to either excessive lead length on through hole parts or excessive tracking on surface mount types. It is more important to have the decoupling capacitor close to the supply lines of the IC it is supposed to decouple, than to the circuit supply inlet.

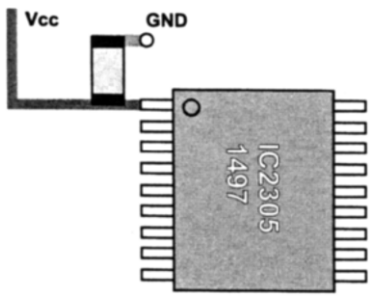

Figure 6.6
Locate decoupling capacitor at IC supply pins

One of the main circuit causes of interference in a digital or mixed signal system is the digital system clock. One way of minimising its break through on the supply rail is to give the clock generating circuit its own decoupling capacitor and if possible a small bypass capacitor. Again these need locating close to the clock circuit and

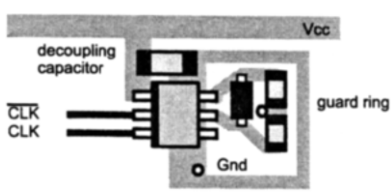

Figure 6.7
Decoupled clock circuit with guard ring

buffers. This whole circuit may benefit from segmenting on the power plane only, the clock and digital grounds should not be segmented. Even filtering may be beneficial on the supply from the digital power supply rail to the local clock circuit. The value of decoupling capacitor will depend to some extent on the clock rate and low values should be used. With clocks up to about 30 MHz a 4.7 nF decoupling capacitor in parallel with a 1 μF reservoir can significantly reduce supply ripple due to the clock and its driver circuit.

6.4.3 Grounding Techniques

This section ties in closely with decoupling and segmentation, but its effectiveness and the techniques available depend very much on the PCB complexity available. The ideal would be to have a multi-layer PCB in which ground and power planes can be defined as separate layers. This can be too expensive for small circuits and there are many single- and double-sided boards that will still need some grounding techniques applied.

The main objective of grounding techniques is to minimise the ground impedance and the size of any potential ground loops from a circuit back to the supply. Note this is not just minimising resistance, at the frequencies of interest for EMC it is inductive reactance of the tracking that usually dominates the impedance characteristic.

One grounding technique that can be used on any complexity of PCB is a guard ring. This is a ground connected track that does not carry a return current for the circuit under normal operation. Its purpose is mainly as a return source for radio-frequency (RF) current that is radiating out of, or incident to, the PCB. It is usually tracked around the outer edge of a PCB, or segments within a PCB, and often around connectors and input–output circuits. If a separate safety earth is being used the guard ring can be connected to this rather than system ground and safety or electrostatic discharge (ESD) devices may sink their current via this track. It is possible to use a guard ring to reduce the segmentation spacing rules as the guard ring can act as a field fringing sink. A guard ring can also be placed around the edge of a power plane as well as tracking layers, this reduces field fringing from uncoupled fields at the edges of a PCB.

On a single-sided PCB, a grounding strategy can still be implemented. The first consideration would be to plan for a wide ground track covering as much of the PCB as possible. Do not attempt a ground plane and then etch out the plane for tracking. This can actually cause more problems than it solves as it may leave unconnected metallised areas within the PCB that can reflect signals through the board or act as receivers and inject capacitively into nearby tracks. A preference for a star arrangement of connecting ground and power should be attempted, but with only a single layer tracking this may be difficult. Definitely apply the segmentation rule of fastest circuits closer to the PSU input to the PCB. Using inductor–capacitor filters at the input to each circuit from a daisy-chained power rail could in fact help with the limited available tracking as the inductors can be used from the supply rail as bridging components. A guard rail can be placed around the edge of the PCB

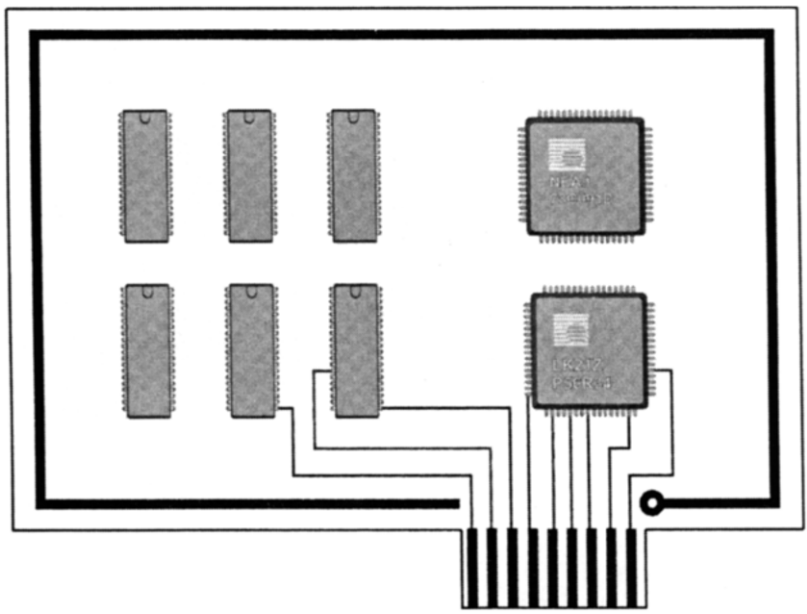

Figure 6.8
Guard ring on component side

connecting to the ground at the input to the PCB only, even on a single-sided board this helps reduce field fringing at the board edge and if a shield becomes necessary leaving the guard ring as uncovered track gives a suitable place to attach the shield.

With a double-sided PCB a ground grid (ground matrix) arrangement should be attempted on digital circuit sections. A ground grid forms a series of box sections on the PCB, which not only reduces the ground impedance but also the size of potential ground loops and signal return loops. A ground plate beneath each IC on the component side will also help even if a full grid cannot be implemented, decoupling capacitors can be tied directly to the IC supply line using this plate. A thick track for the ground grid would be preferred to maintain a low ground impedance, but with high pin count surface mount components this is not always possible. A thin track completing the grid is better than no track as even though this is not a particularly low impedance solution, it still minimises loop areas for both ground currents and signal return paths.

For ground grids to be truly effective at minimising signal loops a similar pattern for the supply should be attempted, mirroring where possible the ground paths. The supply does not have to completely grid in the same way the ground does and comb or star supply arrangements can be very effective coupled with a complete ground grid (comb patterning should not be used on grounding schemes).

With any tracked ground and supply rails, try to track the power rails to mirror the ground, this will increase the effective distributed supply capacitance and minimises

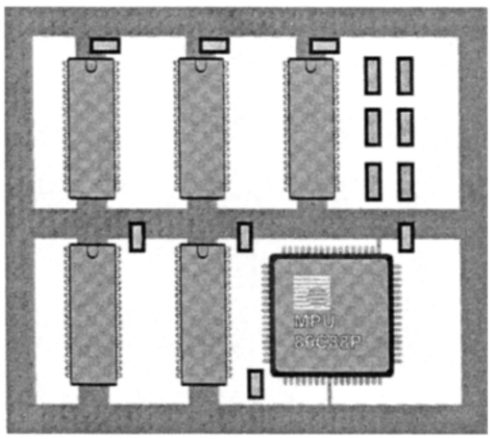

Figure 6.9
Ground grid

the supply-ground loop. Having the supply track slightly narrower than the ground also helps with supply field fringing and reduces cross-talk from the supply rail to nearby signal tracks.

On a multi-layer PCB the ground and power planes should be planned first and usually close together. If one of the supply planes has to be sacrificed for tracking it should always be a power plane, the ground plane should be maintained wherever possible.

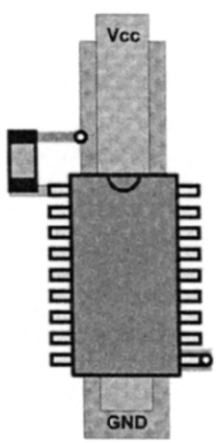

Figure 6.10
Mirror power track over ground track

Many EMC problems encountered with single- and double-sided PCB designs have been solved by simply increasing the PCB stack and including a ground plane. The preferred stack would have ground and power planes separated by a prepreg layer (foil build) or thin laminate, with a thick laminate between power and tracking and a thin laminate between ground and tracking. Using a thin layer between the power and ground planes minimises the distance between these hence maximises the effective capacitance. A PCB capacitor constructed in this manner has a very high-frequency response (high self-resonant frequency) and low series inductance. This construction works as a low value distributed capacitance rather than a bulk single point capacitor. The level of high frequency performance in a distributed plane capacitor cannot usually be found in a discrete component and can be provided by the PCB without adding to the component cost.

Fast circuit signals and sensitive analogue lines should be tracked on the layers closest to the ground plane. The tracking closest to the power plane should be reserved for bias tracks and slower circuits. Using a thicker laminate between power and tracks reduces the capacitive coupling to any signals on this tracking layer, hence reduces the supply cross-talk to these signals. A thin laminate between ground and tracking adds capacitive coupling to the tracks and can allow impedance controlled tracking to be incorporated, but for long track sections or fast pulses this coupling can slow the signal (see section on high speed PCB design).

Again if insufficient layers are available for a separate ground plane, then with sensitive and high frequency signals there should be a ground track beneath the tracking. Producing a ground mirror for these signals ensures minimum loop area, hence minimises radiated signals. For differential signalling the complementary track pairs should be made to mirror each other.

A separate safety ground as either a plane or a guard track is particularly useful where signals enter and exit the system. Often the safety ground cannot be used over a complete PCB plane due to leakage current specifications being exceeded by capacitive coupling effects. A low value decoupling capacitor between signal and safety ground close to the off-board signal connector provides a high frequency

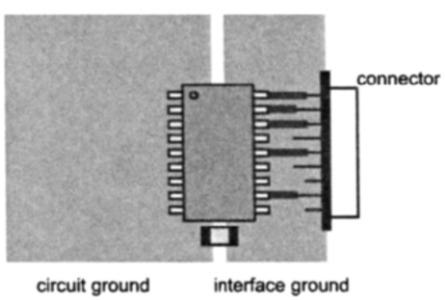

Figure 6.11
Interface circuit ground

current ground link between system and safety references. Capacitive coupling between analogue and digital grounds close to any signal interface (e.g. ADC/DAC) should also be planned to bridge the moat region (the capacitor can always be omitted if not required), again low values of capacitive coupling is required (<1 nF).

PCB structure with many layers and a ground plane can implement several of these rules, including a surface ground grid on digital sections with a buried ground plane and even multiple ground planes. In instances where there are several ground circuits or configurations these need to be interconnected to maintain a low impedance and short return loops. Ground stitching is a technique usually referred to placing multiple vias between ground areas at regular intervals. This can be used with guard rings and large grounded areas on PCBs, which are results of copper fill. If the chassis of the system is also grounded using plated through holes for the stitching points and further connecting these to the chassis can produce very quiet PCB designs even with high-speed digital systems.

Copper fill has been a common technique with some analogue circuits, this technique introduces areas of copper on the surface of a PCB which carry no signals and which should be grounded. Although this has the potential to produce a good overall shield to reduce field fringing and improve decoupling, the copper areas can be left unconnected in circumstances and this can produce induced electromagnetic interference (EMI) problems. This technique is not suitable for digital circuits as it can create differences in signal skew and propagation delay between tracks that lead to functional failures. Consequently, copper fill is not a particularly popular scheme in modern designs and should be used with care on analogue circuits only or avoided altogether.

6.4.4 Order of Layout

Layout of the PCB should be done with a certain order of tracks. PCB layout is usually performed on a computer and it is often left to an auto-router to place tracks when using a CAD system. Unfortunately, few of these CAD systems have the intelligence required to consider the implications of how the routeing may affect the EMC of the end system. Indeed, few will have the necessary links to a simulator or netlist to know which tracks are high speed or which are power rails (see Chapter 8 for discussion of CAD programs for EMC). Consequently, some of the more sensitive and fastest tracks may require a manual routeing before the auto-router can be left to finish off the bias and slow signal tracking.

There are few PCB layout programs that can handle the grounding techniques mentioned above, particularly guard rings and segmentation. EMC considerations are therefore going to reduce the reliance on software in the near future as far as routeing and placement are concerned, and manual layout will be required at least for fast and sensitive signal lines.

If multi-layers or ground and power planes are not available, then ground tracking needs consideration before any other tracks. Ground tracks need to be wide and cover as large an area as possible. The highest frequency tracks then need to be laid out, these should be the shortest tracks on the PCB, hence laying them first gives them priority

and there should be little other tracking to route around. Sensitive analogue signal tracks need laying down next, then other signal and finally biasing component tracks.

In digital systems the clock or oscillator is the track that should be placed immediately after the power rails. The clock is a particularly problematic track as this usually goes to just about every IC in a synchronous system, hence even when laid first may still be a long track. Additional guard rings may be required for the clock if this is a particularly long section of track to reduce fringing and minimise loop area. The lower order address lines between processors and off-chip memory are usually the next fastest signals after the clock, then data lines.

Digital system tracks should be the same length between processors and each target circuit to minimise skew. Clock lines usually contain the highest frequency content so are the most liable to generate emissions, hence these need to be as short as possible and the clock circuit should be close to or even on-board the fastest operating device (usually the microprocessor). Try and maintain all clock signals to one layer, changing layers changes the characteristic impedance and propagation delay for the signal. By laying down these fastest signals first not only are the track lengths minimised (as there are no other tracks to avoid) but also the number of vias present on these signal lines is minimised.

Another order issue within multilayer boards is the position of each layer within the PCB stack. It is always preferable to have the power and ground plane close (as

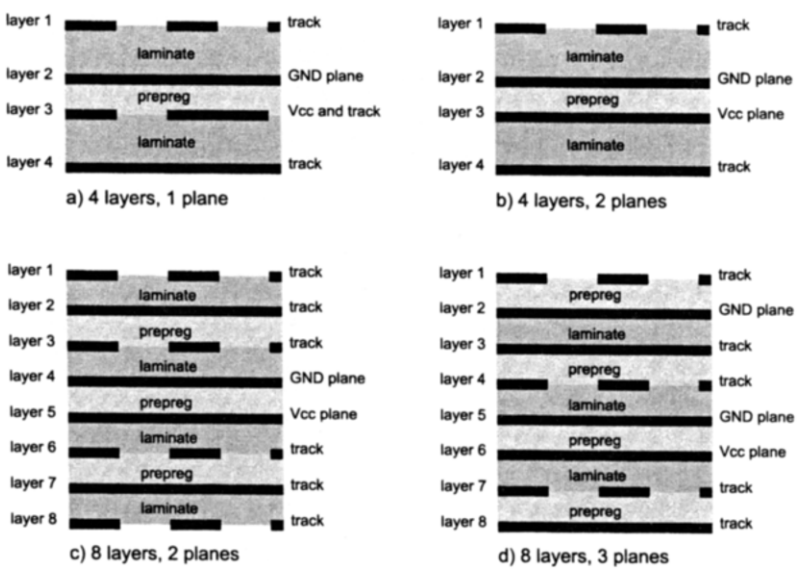

Figure 6.12

Examples of four- and eight-layer track assignments

mentioned previously). The ground should be between the power plane and fastest and most sensitive signal tracks. This may imply having a power plane on an outer layer, which is not always possible due to manufacturing requirements, but could be the quietest solution for a surface mount board with a single component side.

Clock and other high-speed signals should be routed on a layer close to the ground plane. The highest speed signals should track on only one or two layers and these should be adjacent layers. High speed signals should not cross through the ground or power planes if avoidable, this can be achieved with single component sided boards or using multiple layers above or between ground planes. If components are to be placed on both sides and high speed signals tracked through from surface to surface, a second ground plane is probably necessary with the power plane sandwiched between them. Alternatively, a ground mirror track for these high speed signals may have to be patterned between the high speed track and power plane. This mirror track should be three times the width of the signal track to minimise field fringing.

6.4.5 Other Tracking Issues

Where the circuit requires more than one power supply (e.g. ±12 V, or 5 V and 12 V) then these should be patterned into a single layer. If sufficient layers are available to give each supply its own plane then these should be on either side of a ground plane.

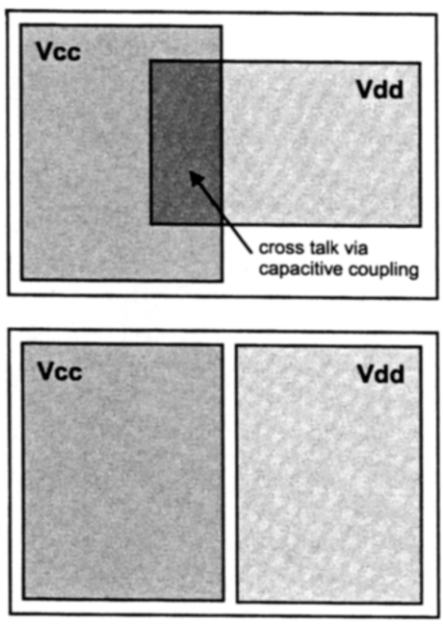

Figure 6.13
Power plane layout

Different supply rails should not be overlapped unless separated by a ground plane, otherwise there is a large potential for coupling, which can upset the system and is difficult to filter. Any overlap of the power planes is a potential cross-talk coupling point between the rails, hence a noisy device attached to one of the supplies is given the opportunity to interfere with any device coupled to the alternative supply rail. A moat separation of about 5 mm should be given between power plane patterns.

To reduce field fringing from the edge of power planes, either single supply or multiple rails, it would also be recommended that the supply plane is slightly inset from the ground plane. An inset of 5 mm gives approximately 60% reduction in field fringing from the edge of the plane.

Where there are two or more tracking layers above a single ground plane cross-talk is minimised by running the tracks orthogonal to one another. Having orthogonal tracks not only helps reduce cross-talk by minimising overlap area, but eases routeing by defining a directional pattern for each layer. Cross-talk is usually produced due to capacitive coupling, so an increase in laminate thickness may help, but this will reduce the effective signal to ground decoupling and change the characteristic track impedance and capacitance.

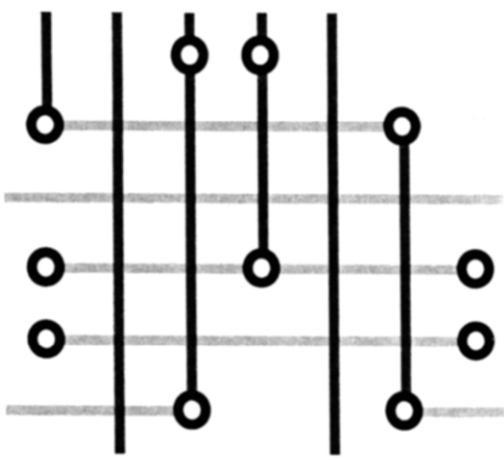

Figure 6.14
Track alternate layers orthogonally

Orthogonal tracking is best suited to lower speed signals, for high-speed signals the discontinuity in the impedance profile of the track, caused by a via, can create reflections and signal loss. The fastest signals should be laid on a single layer and vias and layer changes minimised. A via can introduce between 1 and 4 nH of inductance to a track (depending on via height), with a small capacitive content (0.3–0.8 pF) as the via is perpendicular to any ground plane or ground tracking.

Consequently, vias should be minimised and used sparingly, where unavoidable on high-speed lines the number of vias should be matched on parallel signal lines (i.e. address and data busses).

Where tracks are cornered on a layer, a sharp right angle can produce a field concentration at the inner edge. Although these fields are not strong enough to fail EMC emissions testing they can cause noise injection into other tracks on the PCB. Therefore all corners should be rounded if possible or mitred (angled) by 45°. The radius of bend should be at least twice the track width, or the mitre should contain at least one track width in length along the angled section. Rounded cornering is generally better but not as frequently supported as mitred tracking in PCB CAD packages.

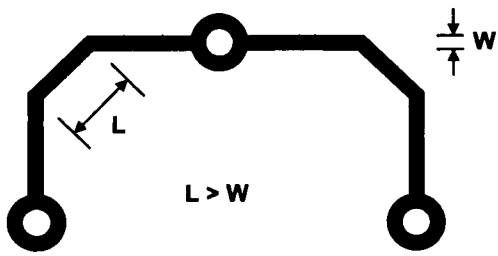

Figure 6.15
Mitre track corners

Right-angled tracking also creates a small discontinuity in the resistance profile of the track (a sharp corner is equivalent to 0.6 of a square of straight track). Although unlikely to cause a reflection in the signal it can make accurate calculation of track resistance awkward.

Avoid producing stubs with tracks carrying high frequency and sensitive signals (i.e. low voltage). Stubs produce reflections as well as potentially adding a wavelength divisible aerials to the circuit. It is not always simple to predict the frequency components in a signal from the simple equations already quoted. So although a stub length may compute to be a non-quarter wavelength integer of any known signal in the system, incident radiation may resonate on a stub.

Another tracking scheme to be avoided is a star signal arrangement where signal tracking radiates from a single point. Although star arrangements are suitable for bonding ground rails from multiple PCBs, with a signal track this introduces multiple stubs. A radiating signal arrangement is usually the shortest tracking and causes minimum delays from source to all receivers, but the multiple reflections and potential for radiated interference create more problems for the circuit's EMI performance.

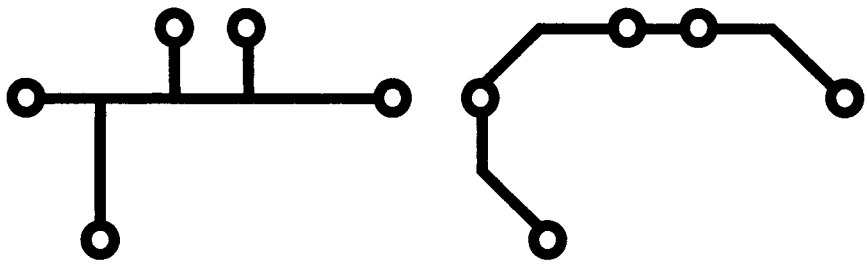

Figure 6.16
Do not use stubs for high frequency tracks

Try to maintain signal tracks at a constant width throughout the length of the track. Varying track width creates changes in track impedance (resistance, inductance and capacitance) and, consequently, the opportunity for reflections and line impedance imbalances. A thin track is less problematic than a varying track. Tracks carrying a bias that is tapped off, and hence can become thinner as they progress, should be funnelled so as to produce a smooth impedance change and remove the possibility of creating a reflection or resonance for interference signals, which are superimposed on the bias.

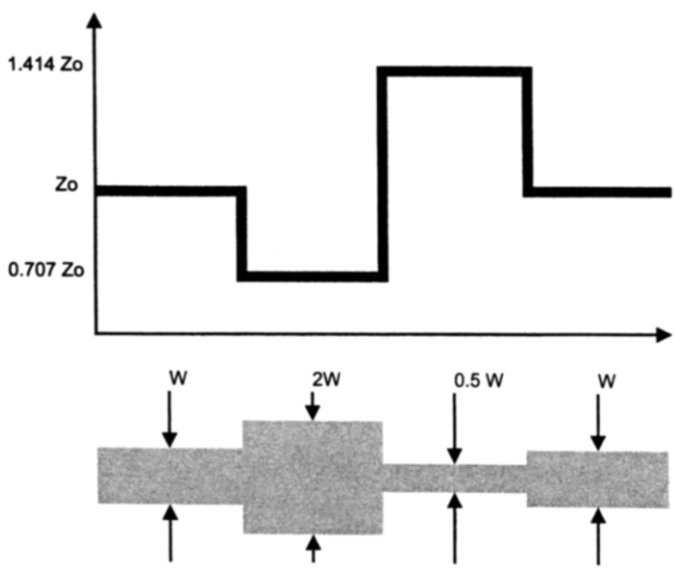

Figure 6.17
Impedance changes with track width variation

Vias and plated through holes in the ground and power planes should be reasonably distributed throughout a layout. A concentration of holes that pass through supply planes produce a localised impedance difference near the holes, hence not only is the area a 'hot spot' of signal activity, but the supply planes are higher impedance at this point and less effective as RF sinks. Hole concentrations cause local tracks to be more susceptible to interference. Where there is a natural concentration of holes (e.g. a through hole connector) the ground plane should surround each hole to minimise local impedance and avoid creating an aperture, this also increases decoupling into the connector or device.

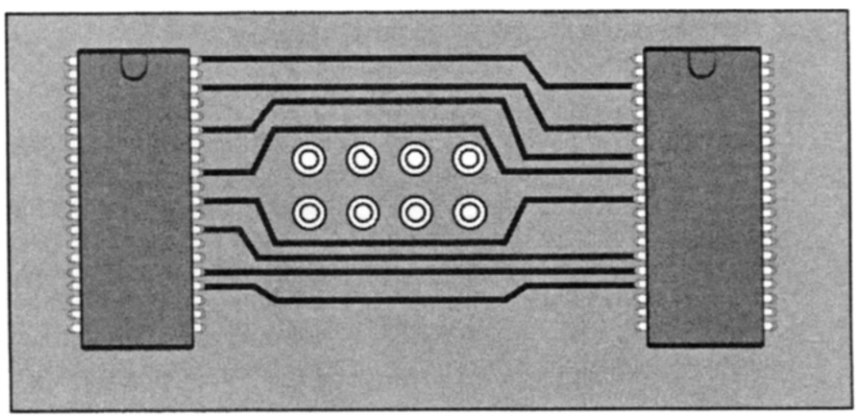

Figure 6.18
Avoid via concentrations

Ground or return signal impedance can also be accidentally increased due to any slits or apertures in the PCB. Apertures should be avoided as they not only increase the ground impedance, but may act as a potential aerial across their length. A series of small holes is preferable to a slit in a ground plane as even though the impedance is slightly increased it is not as problematic as a slit aperture.

Do not deliberately create split apertures (i.e. long holes or wide vias) in power and ground planes. These create an area of non-uniformity within the planes and reduce their effectiveness as shields, as well as locally increasing the impedance of the power and ground planes. This type of feature is usually only required by cabling and cabling should not be brought through a PCB. If the feature is required due to mechanical constraints within the completed system (i.e. physically has to fit over a shaped object) then maintain a ground plane around the aperture and guard rings should be provided on tracking layers.

Do not leave any unconnected metallised patterns. If components have a pad which is not connected (often marked NC on the pin-out or schematic diagram) but soldered down, connect to the ground. If the pin is suspected to be internally

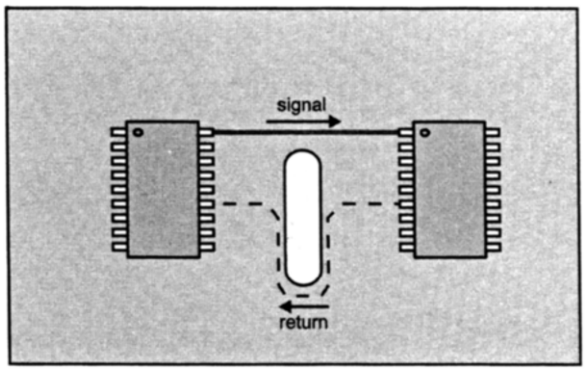

Figure 6.19
Avoid slit apertures in the PCB

connected contact the supplier for confirmation, otherwise route to a convenient point. Unconnected metallisation can act as an aerial and inject into the local circuit capacitively. Often unconnected metallisation is used for thermal dissipation of the device within the package, hence grounding is the best method as the ground plane/track should have the highest amount of metal to act as a heat sink. Always check the data sheet or call the manufacturer if unsure.

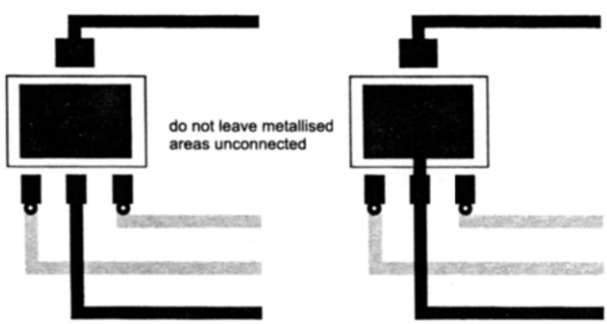

Figure 6.20
Connect all metallised areas

Minimise loop areas by keeping tracks to and from components and sockets close together (signal and returns). This reduces the potential aerial loop size and the capacitive coupling between these tracks minimises bandwidth. With high speed single-ended signals sometimes the ground return may also have to be tracked alongside the signal if the signal does not track over a low impedance ground plane.

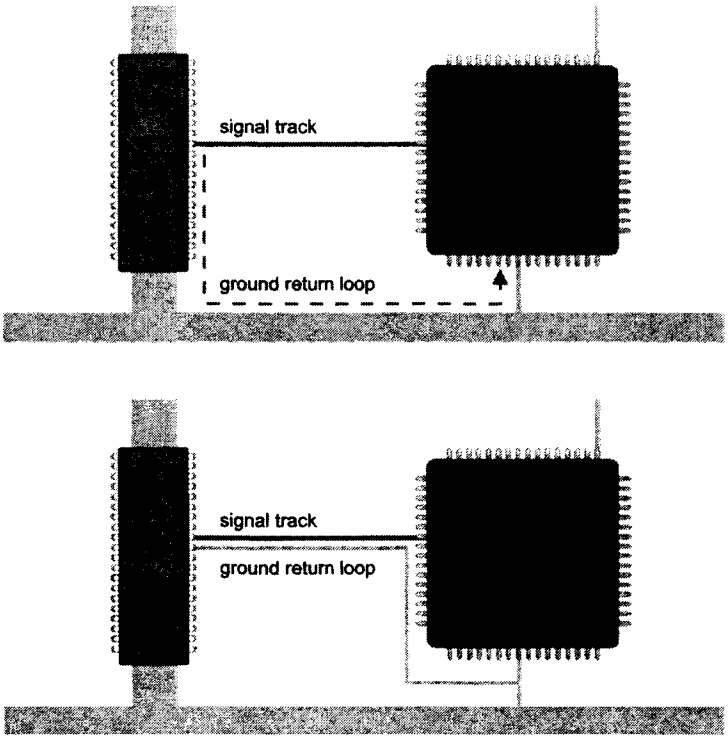

Figure 6.21
Minimise return loop area

Many of the tracking issues may seem trivial, they may appear not to be likely sources of emissions from the system. It is not just emission out of the system that could be the ultimate problem, but emissions within the system causing internal interference or injecting back into the circuits to produce conducted noise. Consider an unconnected metallised area for a small component back plate, a SOT223 transistor for example. The metallised plate will reflect any incident radiated field, and rotate the field through 90°. If the incident radiation failed to interfere the first time it passed through a local component, with its plane rotated the radiation gets a second chance, it may even be rotated to pass through the plane of the PCB itself. Although individually each idea presented here may produce a negligible influence on the EMC of a system, it is the sum of many of these design principles which can reduce both emissions and susceptibility of the completed design.