CHAPTER 4

INTEGRATED CIRCUITS

As the complexity of integrated circuits (ICs) increases, so does their ability to influence the electromagnetic compatibility (EMC) of any given application. Often there can be benefits as the closer proximity of components integrated into the silicon, shorter lead lengths (measured in microns rather than millimetres) and embedding of functions reduces the opportunity for radiated emissions and limits the power supply variations to within a few devices. There are downsides as well, as any problems that do occur are next to impossible to fix unless they present themselves for remedy on the device pins; also higher power requirements in a single device can produce greater current demand down a single printed circuit board (PCB) trace.

It could be argued that most of the electromagnetic compatibility (EMC) issues within ICs have to be dealt with by the IC circuit designers and IC suppliers; however, they may not be using or designing the device for the application you are attempting to produce, in fact you may be their only customer using the device in such an application where an EMC problem has occurred. Either way there are still a few basic EMC design issues that can be applied to even the most complex ICs to minimise the possibility of producing a poor EMC performance.

4.1 Bipolar or CMOS?

There may be a choice of semiconductor technology for certain IC applications, as combinational logic devices are available in various types of bipolar and CMOS processes. The majority of digital ICs are nowadays manufactured in CMOS with many analogue ICs following and except for specific application areas bipolar is certainly losing popularity. Mixed technology (BiCMOS) is gaining popularity in certain linear and mixed signal (digital and analogue) circuits and in ASIC designs. Unless specifically dictated by the circuit function, opting for a bipolar or unipolar technology will effect the EMC performance of a circuit.

The benefit is not always obvious, for example CMOS may not necessarily have the lowest power consumption as is often assumed. Bipolar can be run at very low-voltage levels, hence low power and does not have the switching power overhead of some synchronous CMOS devices. Static power consumption of CMOS may be lower, but at fast clock rates each CMOS IC introduces a large power demand on the

supply. The power consumption of a clocked synchronous CMOS device is therefore dependent on the system clock frequency and device loading, at high frequencies the dynamic power demand of a CMOS IC may exceed an equivalent bipolar device. Consequently, at high switching speeds, it may be preferable to have bipolar circuits to reduce the conducted noise in a circuit and limit the amount of decoupling capacitance required.

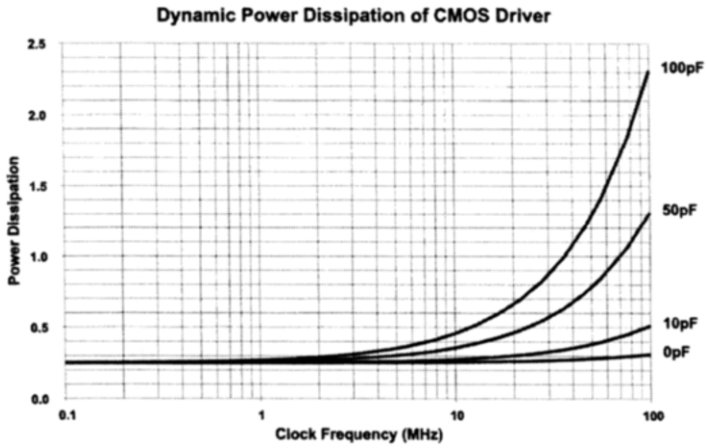


Figure 4.1

Change of CMOS dynamic power dissipation with capacitive load

The main downside to bipolar technology is its ability to demodulate radio-frequencies (RF). Both unipolar and bipolar devices can demodulate RF radiated fields due to the non-linear voltage–current relationships of the transistor structures. Unipolar has a square law dependency and bipolar an exponential law dependence and consequently produces a much better demodulator. In discrete circuits the demodulation is limited as even the smallest discrete device has a relatively large junction area, hence can demodulate only limited RF. Additionally, discrete circuit interconnect (PCB traces) often filters the signal from being conducted from a discrete device and being amplified within the rest of the circuit. In an integrated circuit the transistors have extremely small junction dimensions and interconnect between components is short, the demodulated signal can therefore be amplified within the IC. This is one method that RF can become injected into circuits, via a susceptible IC. The RF carrier itself appears as a DC offset on the susceptible signal, the demodulated signal could be anywhere in the frequency spectrum depending on the source. Common occurrences are audio frequencies from demodulated telecommunications and/or radio signals.

Examples of demodulated RF do exist, well known examples occur in professional audio circuitry (e.g. taxi radio broadcast pick-up on public address systems) and the

effect is certainly more noticeable in audio analogue circuits. In digital systems the effect is less noticeable but could still upset system stability, the DC offset in particular can affect logic transition timing between susceptible and immune ICs. The effect of DC offset will be particularly problematic in low-voltage digital systems where even seemingly small DC offsets can produce signal jitter and instabilities, creating signal integrity and timing problems. The effect will be more problematic the faster the system clock rate and the faster the capability of the base logic used.

4.2 Integrated Circuit Packaging

ICs have almost as many package styles as they do functions. One common factor in most package styles, whether through hole or surface mount, is the assembly of the IC into its package. The IC is placed on to an island within the body of the package, the island is often attached to the lead frame in plastic-moulded packages or to the base material in ceramic packages. Bond wires are attached between each device pin and the IC bond pads. Although the leads from the package to the IC can be of differing length depending on their position at the package outline, the bond wires tend to be of very similar lengths, hence add a similar amount of inductance to each lead.

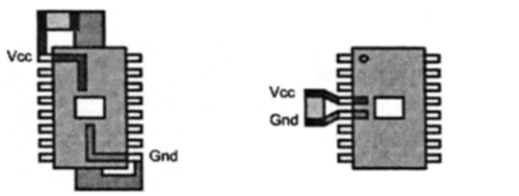
As with discrete packages the bond wire parasitic inductance is about 0.5 nH. Package inductance varies from pin to pin between 2 nH for shot central pins up to 10–20 nH for end pins in large DIL packs (e.g. 40-pin DIL types). Package capacitance varies by a similar amount, about 0.4 pF being a typical low value for short pins with about 1 pF for the longest types. Although there is some variation between plastic and ceramic material with regards to their dielectric properties, due to the dimensions and low values involved these differences appear insignificant in affecting the parasitic lead capacitance or inductance (Table 4.1).

Table 4.1 *Typical lead parasitics of IC packages*

Leads	Dual in-line (DIL)		Small outline (SOIC)		Plastic leaded chip carrier (PLCC)	
	L (nH)	C (pF)	L (nH)	C (pF)	L (nH)	C (pF)
8	6.3	0.68	3.1	0.35		
14	6.7	0.74	3.2	0.36		
16	6.9	0.77	3.4	0.38		
20	8.6	1.01	6.7	0.65	4.6	0.62
24	9.1	1.06	7.2	1.14		
28	9.6	1.14			5.8	0.72
40/44	11.0	1.25			5.9	0.77
64/68	17.6	1.51			6.1	0.80

As usual surface mount is the preferred style for EMC performance due to lower package parasitics. There is also reduced loop area with surface mount packages, particularly with quad flat packs (QFP). Some quad flat packs can offer 66% less loop area between trace pairs than comparable dual in-line package styles. Recent package styles, such as ball grid arrays (BGA) and tape automated bonding (TAB), can reduce package parasitics further due to reduced lead lengths and no bonding wires.

Even within a given package type there are EMC benefits to certain assignments of the pin connections. With DIL style packages for instance the pins closest to the centre are the shortest, hence these are the best pins to use for the supply lines (lowest lead inductance). Also packages with supply lines on adjacent pins make decoupling capacitor placement easier. The same arguments can be applied to other package styles, with the power supply rails and then the fastest signal traces requiring the shortest pins.



a) large loop area for supply and decoupling capacitor

b) reduced loop area and closer location of decoupling capacitor

Figure 4.2
Dual-in-line power supply loop area

4.3 Digital Devices

Many people believe that using a digital circuit, rather than an analogue solution, can circumvent some of their EMC problems as RF and EMC are considered analogue topics. Unfortunately, this view is very misguided, as one feature prevalent in digital circuits, sharp edges and square pulses, can generate a large amount of electromagnetic interference (EMI) with a large harmonic frequency content.

There is a lot that the designer can do with many digital circuits for minimising EMC problems, such as filtering and slew rate limiting, even when sharp edges and fast rise times may be inherently required for circuit functionality or are a feature of the devices in use. There are tricks and techniques that are useful to know and if a choice appears between a potential EMC threat and a potentially benign component, some background knowledge can help make the appropriate choice.

The main considerations are going to be based on the operating speed and rise or fall times of the digital circuits (it is mainly the rise times as most digital circuit transitions occur on the rising edge of the clock signal). The equation for use in

estimating the potential harmonic threat of sharp pulse edges was introduced in the capacitor section. The equation gives the harmonic frequency content (f_{edge}) of a pulse with either a fast rise (τ_r) and/or fall (τ_f) time:

$$f_{edge} = \frac{1}{\pi\tau_r} \text{ or } f_{edge} = \frac{1}{\pi\tau_f} \quad 4.1$$

This equation should be used to determine the frequency response required for decoupling capacitors (see capacitor section) and can be used to determine worse case tracking lengths when laying out a PCB. There could still be harmonic content present at up to 10 times this frequency if the signal is particularly square and overshoot and ringing could add additional harmonic signature.

The above equation will really only begin to predict the significant harmonic content from edges when rise and fall times exceed 10 ns. This generally occurs when clock frequencies exceed 10 MHz and by the time 50 MHz clocks are used the equation becomes essential to predict harmonic content. One problem of gauging the necessity of the equation is that many digital IC specifications only quote maximum rise or fall times. As far as EMC performance or problems are concerned the designer rarely knows the worse case conditions from the IC in use (i.e. the minimum rise/fall times). For example HC CMOS has a quoted maximum rise time of 10 ns, in reality 4 ns is more typical, which means that a logic capable of being clocked at a maximum of 32 MHz could introduce harmonic content up to 80 MHz into its signals.

Some digital designs can avoid many of the problems associated with these edge harmonics by having a level triggered design (i.e. trigger only when the clock is at a stable level rather than on a rising edge). As well as the high harmonic content of the transition, clock edges are also relatively noisy due to being connected to multiple devices switching all at the same time affecting the shape of the edge. By having a logic design that worked on stable levels, the effect of the edges on the circuit functionality is minimised and although the radiated and conducted emissions may be unaffected, the circuit itself is less susceptible. Level triggered logic is not as popular as edge triggered as it isn't quite as easy to implement, hence although a nice idea from an EMC standpoint, it can be impractical in many circuits due to the availability of level triggered ICs.

Owing to the threshold of the switching levels involved in digital circuits (typically 100 mV to a few volts) the components tend to have an inherent level of immunity to EMI that is not always possible with an analogue circuit. The high-voltage swing of both signals and clock edges, at relatively high rates does increase the potential emissions compared with a continuous analogue signal.

4.3.1 Clock Circuits

Potentially, clock circuits are the greatest EMC threat in a system. This may be somewhat unfair as it is not always the clock that causes the problem, but the circuits it tries to drive, including the PCB layout to these circuits. However, the most

common noise problem from a digital circuit, either conducted or radiated, usually occurs at the same frequency as (or a discrete harmonic of) the clock.

There are some specific layout issues which are covered in the PCB section, but good grounding and adequate decoupling are two items that cannot be reiterated enough. Often other good EMC design practices are ruined due to simple errors in ground systems or inadequate decoupling. Additionally, a small bypass capacitor should be located with the clock driver circuit to reduce its load to the supply; a value as low as 100 nF should be adequate for most oscillators and resonator circuit supply lines.

It should not need stating that a designer should use the slowest clock speed possible, this is a general statement for any switching or logic device. If available use primary crystals or oscillators, derived or divided frequency parts will have the primary crystal frequency superimposed on the clock as well as the power line, which introduces unnecessary additional high frequency components of noise with much higher spectral power in the harmonics than would occur with a slower primary clock.

Slew rate limiting the clock is desirable, most logic ICs have a clock buffer on board and the slew rate-limited signal will be reconstructed as a square wave at the IC interface. Slew rate limiting only becomes a problem if using mixed technology logic ICs (e.g. CMOS and TTL) which have different switching thresholds. The threshold level itself is not the problem but the fact that the devices can have a slightly different switching point in time from the same clock edge. There are instances where the offset switching points can lower emissions, as the transitions cause a spread of power demand, similar to spread spectrum techniques (see below). Spread spectrum clock and spread spectrum device switching are, however, not the same and the latter can cause functional problems (signal integrity) and jitter on signal lines. Although slew rate limiting is a good idea in itself for reduced conducted emissions and reduced harmonic content it should be avoided with mixed logic types (although avoiding mixed logic families is preferable).

Limiting the available current drive to the known fan-out count also helps reduce noise problems, if available low output drive parts should be used. Overdriving the clock line wastes power and this power will inevitably find its way into noise or heat, causing a problem somewhere in the circuit. Distributing the clock to high impedance local buffers can also help as low circulating currents are distributed around the circuit with higher current demand localised to each sub-system or functional area. The clock line will need to be matched to the receiving line and terminating circuits may be required, but this should reduce reflections and ringing and hence overall EMI.

Dedicated clock driver circuits can also help in reducing the noise caused by clocks. The easiest example to consider is the multiple clock gate output circuit, this provides sufficient independent drivers and allows several independent lines to be driven. This arrangement permits each individual line impedance to be matched and reduces the possibility of cross-talk from one clocked line interfering with the other lines. A set of independent clock drivers with line-matched impedances also reduces

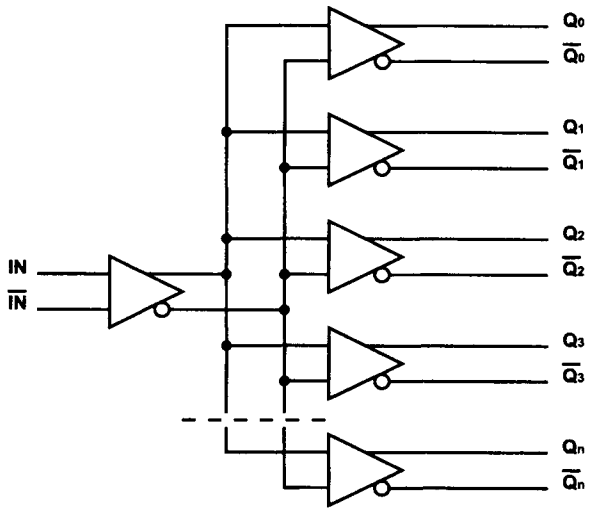


Figure 4.3
Clock distribution buffers

the possibility of clock skew at circuits furthest from the clock generator, and hence helps maintain functional synchronicity and signal integrity across the system.

A new approach to reducing emissions from the clock is the spread spectrum clock (SSC). This device gives a small spread in the absolute frequency of the clock by a few per cent centred around the fundamental clock frequency. Spreading the clock by a few per cent does not cause a problem with digital circuitry as the differences are only a few per cent and all devices see these small shifts at the same time, and hence remain synchronous. The overall system speed is unaffected as the time average is the same as the fundamental frequency. The advantage of this technique is that it reduces the amount of power at the absolute frequency by about 10 dB (again calculated as a time-averaged value), but incident power at any given moment in time remains at the same level as with a standard clock. The disadvantage is that there is a slightly wider range of frequencies being injected into the system, not only around the fundamental frequency but also around its harmonics. Feature sizes which will resonate at these small frequency changes can become problems that were not present with the original clock frequency and harmonics. The fundamental harmonic content average power is reduced, but edge rate harmonics are unaffected as the rise and fall times of the original clock are maintained.

One of the most useful types of driver or local buffer arrangement for reducing EMC on high-speed clock signals is the phase-locked loop (PLL) buffer. The PLL circuit can be used to synchronise two clocks if necessary, but more importantly from an EMC viewpoint the PLL allows a low speed, and even slow rise time, clock signal to synchronise a faster local clock. Using this arrangement allows a low speed signal,

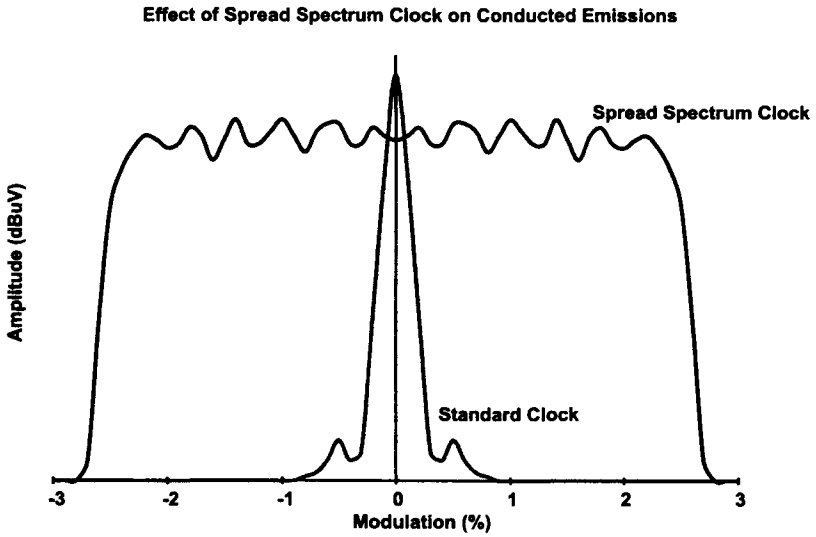


Figure 4.4
Spread spectrum clock emissions

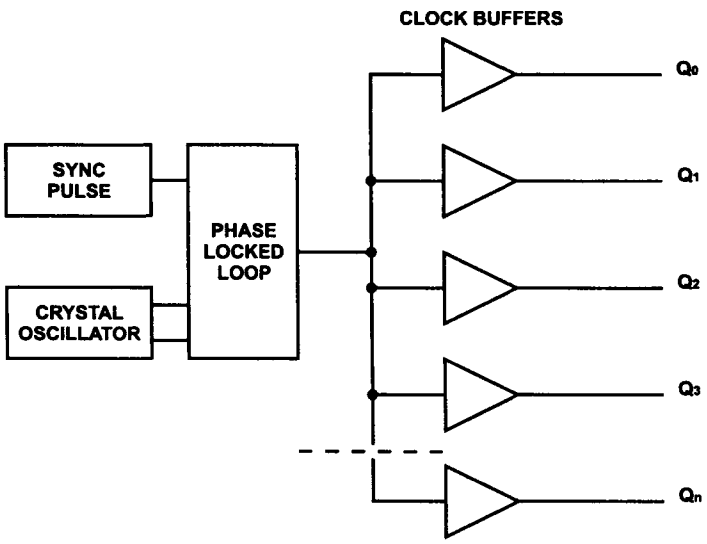


Figure 4.5
PLL synchronisation

say 1 MHz, to synchronise a series of circuits operating locally with a high speed clock, say 50 MHz. The advantages are relatively obvious, a low speed distributed synchronising pulse means that the longer tracks carry only the slower speed signals, whereas each circuit has localised short tracks carrying the faster busses and local high speed clocking. The major drawback is the additional cost of adding PLL devices to each circuit board or the complexity of design involved in adding a PLL circuit to a local programmable device or ASIC. There are many PLL circuits available that can synchronise high speed clocks on quite slow synchronising pulses and the idea should be borne in mind when using a multitude of processing circuits in the same system and requiring synchronisation between the circuits.

4.3.2 Combinational Logic Devices

This is probably the area of digital circuit design where a designer can most actively affect the EMC performance of the circuit. Combinational logic circuits are nowadays used mainly for what is termed as 'glue logic', that is to interface small sections of digital circuits together, either producing address decoders, bit counters or peripheral functions not directly available either in software or on a single IC, and where programmable logic is either too complex or too expensive. Usually, a relatively large amount of tracking and interconnect is required on the PCB considering the level of the function, and the designer has a range of logic families to choose their components from.

There is one base rule for choosing the appropriate logic family (as with all digital circuits), that is to use the slowest type suitable. This is a good rule of thumb and should be borne in mind during all component selection; however, there is a caveat in that the noise margin also significantly affects the EMC performance from a susceptibility standpoint. The lower the noise margin, the more susceptible a component is to external noise and triggering on EMI. Consequently, two families stand out as being especially good from an EMC viewpoint, CMOS and HC CMOS. There are additional design benefits from using these two types of logic, both are low power consumers, hence switching power demands on the supply are very light especially compared with TTL and LS types. It is also possible to run the CMOS and HC CMOS down to a 3.3 V supply rail, hence this type of logic gate can be used, unmodified, with the latest generations of low-supply voltage microprocessors.

There is of course a downside to all situations involving EMC where it appears you have a clear winner! The CMOS devices are more static sensitive from a handling viewpoint than the bipolar technologies (TTL, LS), but as most microprocessors are manufactured in CMOS processes this should not require additional precautions to a manufacturing line's existing electrostatic discharge (ESD) requirement. Of course the operation using CMOS is limited to clock rates of up to 6 MHz and up to 32 MHz with HC CMOS, so the range of applications can seem quite limited when processors with clock speeds exceeding 200 MHz are commonplace.

When using combinational logic in a circuit it should always be of the same family. Mixing logic families can cause excessive skew and jitter on clock lines and

additional harmonics on signal and power lines. There is a potential for functional failure as well as increased harmonics when mixing combinational logic. From a susceptibility viewpoint the circuit is only as immune as its weakest component, using all HC CMOS with a single TTL gate still only provides the same level of immunity as the TTL gate can tolerate (a 0.4 V noise margin compared with 1.0 V for HC CMOS).

Table 4.2 *Comparison of common logic family parameters*

Logic family	Rise/fall time (ns)	Bandwidth (MHz)	Noise margin (V)	Decoupling capacitor (nF)
CMOS	100	6.3	1.0	0.47
LTTTL	20/10	20	0.4	0.33
TTL	10	32	0.4	2.2
HC CMOS	10	32	1.0	0.33
LS	10/6	40	0.3	3.3
ALS	4	100	0.4	2.2
S	3/2.5	120	0.3	1.5
F	1.75	180	0.3	1.5
ECL-10K	2	160	0.125	0.22
ECL-100K	1	320	0.125	0.22

Immunity can be improved in many combinational circuits simply by having all unused pins tied high or low, usually via a resistor. This is especially true of input lines, which can be left open but affect the functionality (e.g. ENABLE, PRESET and CLEAR lines). When logic lines are unterminated the inputs often float at approximately half the supply line, reducing the noise margin by half in many cases as the voltage excursion required to change state is halved. If a further DC offset is added, due to incident RF demodulation for example, the actual noise voltage required to trigger a pin could be only a few tens of millivolts. To minimise power consumption due to the termination the unconnected pins are usually tied to the ground rail via a high value resistor (4.7 kΩ for example).

4.3.3 Microprocessors

There are many types and designs of microprocessor available and not all the ideas given here are applicable to all variants. In particular there may be further techniques available to microcontroller types with on-chip memory and interface functions which are not covered in this section. When using microcontrollers or embedded microprocessors with other on-board functions, also check the section covering the additional on-chip functions discussed here as separate IC devices (e.g. memory, analogue-to-digital converters or ADCs).

Using the minimum clock speed processor is usually possible in applications where the device is being used as an intelligent controller, rather than in base computer designs (i.e. general purpose or personal computers, PCs). This is possibly a bit of an obvious choice as slower processors are usually also the lower cost types. The choice of processor speed may not always be easy to determine as some manufacturers may be selling faster versions, to shift off stock, under the slower version label as these faster devices meet the specification of the slower product. Another possible problem in trying to use a lower speed design is that many processors are being reduced in size by the manufacturer to achieve higher part yield per silicon wafer. Reduced feature sizes usually translate to faster transistors; consequently, although the processor clock rate may not increase, the rise and fall times may be increased and the harmonic content would therefore move up the frequency scale. Many of these changes may not be notified by the supplier, hence a microprocessor may initially be fine, then sometime during its production life cycle begin to suffer EMC problems. Although the part is still sold to the same specification, still labelled and packaged the same, internally the rise times have decreased and subsequently high frequency noise levels and susceptibility increase. If possible, and a higher speed processor is available, it is useful to try the faster device in the design with the lower clock rate to assess how faster rise/fall times will affect the circuit's overall EMC. If the PCB layout and other component guidelines are followed this will hopefully not be a problem.

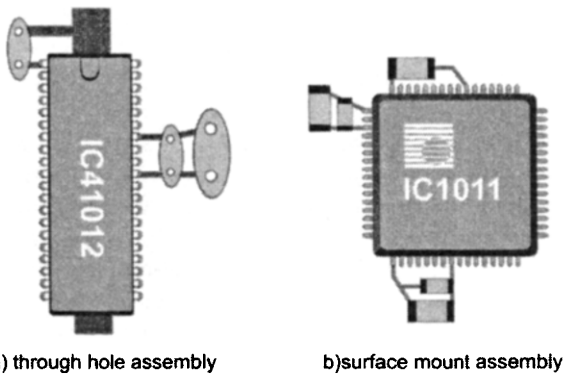
Many applications may not have the option of using slower microprocessors, particularly where real-time operation is involved or where processing speed is an important factor. There are still many ways to reduce the potential for EMC problems.

Microprocessors with off-chip cache need to be sited very closely to the cache device, likewise with co-processors. The microprocessor and off-chip cache and co-processor communicate at very high rates, hence the PCB tracking length needs to be minimised to reduce radiated noise. Any clock circuit should also be sited close and all these ICs will need decoupling capacitors.

The electrical power required by microprocessors is increasing as their processing power increases and it is not uncommon to require a supply function (a regulator for example) very close to the microprocessor IC, with a separate bypass capacitor to reduce its effect on the DC supply to other circuits.

Microprocessors and other ICs which have multiple supply lines, either multiple voltage rails or multiple rails connected internally and/or on the PCB, should have a separate decoupling capacitor per power pin. The value can be quite low, say 4.7 nF per pin. If multiple ground rails are also available tie these together directly to the ground plane and/or place a ground image plane (covered metallisation) on the surface directly below the IC, this reduces ground impedance and radiated noise at the IC.

Where available a microprocessor which will generate the clock on-chip from an off-chip crystal or oscillator is usually preferred to a separate clock driver circuit. The processor is usually the highest power demand device at the clock frequency, hence locating the clock close to the processor ensures minimum drive demand at the clock



a) through hole assembly b)surface mount assembly

Figure 4.6
Multiple decoupling capacitors

frequency distributed around the PCB. This also reduces the chance of noise corruption mis-timing the microprocessor. Noise on the clock will cause more serious problems to the processor than to any other circuit in the majority of designs.

As with most digital devices, pins which are input or mixed input/output are usually high impedance pins. These pins often either float to the mid-point of the supply rails or to an undefined voltage due to internal leakage paths. Either way high impedance pins are susceptible to noise and can register false levels if not properly terminated. Pins which are inputs and are not internally terminated, or terminated via externally connected ICs, need some high resistance (say 4.7 kΩ or 10 kΩ resistor) attached to each pin and ground to ensure a known state is present. This is particularly true of interrupt request (IRQ) and reset pins as a false condition on these pins due to noise will have a catastrophic effect on the circuit behaviour. A higher current consumption is often observed, particularly in CMOS devices, when input pins are unterminated as the input latch is half open, half closed resulting in a leakage current internal to the IC. Terminating high impedance input pins can therefore lead to a reduction in supply current, another benefit to both EMC and functionality.

Owing to the effects that interrupts have on microprocessor operation these are one of the most sensitive pins on the device. The IRQ could also be polled from devices at a distance to the microprocessor on the PCB, or even on a plug-in adapter or subsystem cards. Consequently, it is important to ensure that any line connecting to an interrupt request is protected against ESD transients. If possible a microprocessor should have level triggered interrupts as these are less sensitive to noise and, unless deliberately synchronised for a specific interrupt function, do not have to be synchronous with the clock. Bi-directional diodes, transorbs or metal oxide varistor terminations on the IRQ line are usually adequate for ESD and will help reduce overshoot and ringing without producing a significant line load. Again resistive termination will also maintain the IRQ line in a fixed state when not being polled.

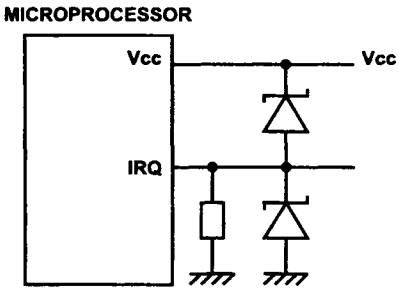


Figure 4.7
IRQ bidirectional diode protection

The microprocessor may be connected to a line driver for its bus interfacing. The bus is the second most likely source (after then the supply line) of an ESD transient reaching the microprocessor, and consequently if the micro is directly connected to the bus ensures that adequate ESD protection is provided at these connections. If the processor does not have adequate protection on-board then use ether a protected buffer as an intermediate interface or a bus protection diode array. The protection should be close to the bus lines rather than the processor itself. This type of protection makes commercial as well as EMC sense as usually the microprocessor is the most expensive component on a PCB, several hundred dollars of microprocessor can be protected for a few cents worth of diodes.

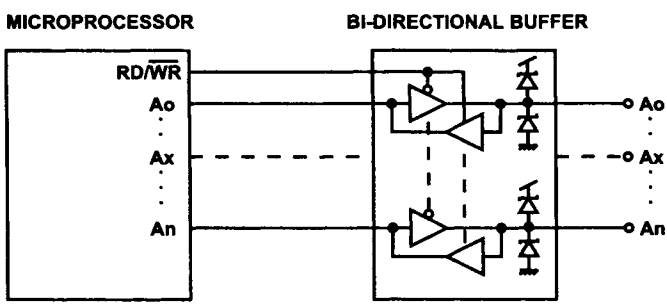


Figure 4.8
Bus buffer with ESD protection

4.3.4 Watchdog Circuits

A watchdog is a circuit which monitors the status of a digital line to determine if the system has crashed or gone into a closed loop. The circuit is usually used with microprocessor or microcontroller circuits where the processor is monitored for either a hardware or software crash (see Chapter 8).

The circuit works as a hardware timer, requiring a clock signal for timing and the monitored line to perform the counter reset before it times out. When the watchdog reaches a time out condition the device is made to poll the reset line of the microprocessor or digital circuit being monitored. Setting the watchdog time-out period is a difficult task and will depend on the system application, times between 10 ms and 2 s are common.

The watchdog circuit does not actually improve the immunity or susceptibility of a digital circuit, but can achieve a controlled recovery if the system is crashed due to an ESD transient or other EMI-related noise signal putting the system into an undefined mode of operation. The watchdog circuit is a safety feature for system recovery in the event of immunity problems, this is still useful in the case of excess EMI from environments the system is not intended to operate in (e.g. lightning strikes, short circuits on peripheral PCBs).

Microprocessors with on-chip watchdog timers are potentially the easiest to operate, all that is required is a few lines of additional code to handle the timing program and set the necessary counters. Some microprocessors can have the watchdog function programmed on-chip if a free running timer is available, and adequate reset programming is added to the code.

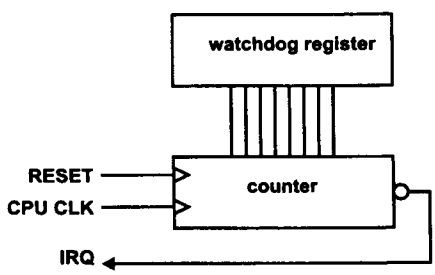


Figure 4.9
On-chip watchdog counter

Unless provided with an on-chip watchdog function, most circuits and microprocessors will require some programming and an output pin dedicating to the watchdog update. A weakness of external watchdog circuits is that they assume the error occurs within the microprocessor or digital circuit being monitored. An excess EMI problem causing false triggering on the clock could cause watchdog resets or false clocking (i.e. EMI problem with the watchdog itself). The watchdog could time-out faster than predicted whereas the digital circuit being monitored (the microprocessor) may in fact be immune to these noise problems due to other EMC protection measures.

Watchdog ICs are available as discrete functions with either programmable or fixed time-out periods. The circuit could also be produced using a simple divider circuit

with a reset line. Watchdog circuits should be made as robust as possible so software programmable types are not recommended for ultimate robustness as their program could also be corrupted and produce false watchdog resets. The trigger for the watchdog toggle (clock) does not necessarily have to come from the system clock, in fact in most instances a slower toggle speed is preferable. The advantage of a slower toggle for the watchdog is that the toggle line could be filtered against high-speed transients with a simple low pass RC or LC filter without affecting the system clock.

Another feature which is advantageous to watchdog circuits is a fixed output reset switch (latch). If the reset line is tied to the main system clock rate, the duration of the reset in a noisy system may not be sufficient to activate the microprocessor reset line. A latched output reset arrangement will, however, require that the reset condition is acknowledged by the microprocessor and the watchdog is then also reset. If a feedback to reset the watchdog is not initiated then the microprocessor immediately sees a reset again after it has restarted.

An alternative to the feedback method is to have an astable output from the watchdog, this is easily and readily achieved when a standard divider circuit is used. In this circuit the astable output reset line from the watchdog is continually toggled high and then low until the microprocessor has restarted. The reset line will actually hold-off the start of the microprocessor for a fixed period (usually the time-out period) until the line is toggled and the processor can restart.

A level sensitive watchdog circuit has the advantage of a higher immunity to clock noise than edge-triggered devices; however, the disadvantage is if the watchdog is monitoring a signal line which has stuck in fixed state. On an edge-triggered watchdog reset this would not cause a problem as the timer would only be reset on the edge and would time-out as usual. With a level triggered watchdog a fixed reset level will prevent the watchdog from resetting the microprocessor, and hence the reset to the watchdog must be AC coupled to the monitored signal.

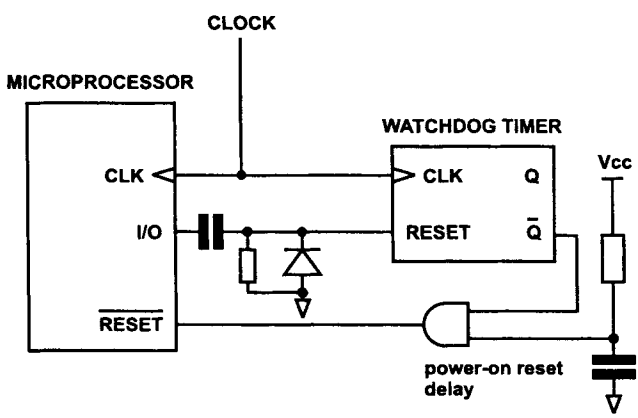


Figure 4.10
External AC coupled watchdog circuit

A good solution to the watchdog function is to use a dedicated output port of the microprocessor and add code to the system to set and clear this as the program progresses. This should then be coupled to the watchdog reset line via an AC coupling circuit. The advantage here is that the system itself requires two commands to reset the watchdog, both a set and clear, hence if a loop error occurs which includes only one of these commands the watchdog will still operate effectively.

The watchdog circuit is often forwarded by microprocessor suppliers as a way of designing for EMC, but it must be remembered that they do not improve the actual circuit EMC performance. Errors which are caused by software problems or hardware faults can also cause watchdog resets, so the circuit is not exclusively an EMI protection device. The benefit of the watchdog circuit is that the system should not get into a catastrophic mode of operation if an error does occur (EMI, hardware or software error), but will recover into a known reset condition (see Chapter 8 for further discussion). The watchdog circuit can also be combined with power-on reset delays, supply drop-out reset and other system reset functions with no additional program overhead as all these functions have a recovery cycle, which is in fact a program or system reset.

4.3.5 Programmable Devices

There are many programmable devices on the market today which are best addressed via other sections within this chapter. For example, one-time programmable (OTP) microcontrollers are covered by the notes on microprocessors. Programmable logic arrays (PLA) and field programmable gate arrays (FPGA) are probably best addressed via the combinational logic section.

One additional feature that some designers incorporate into programmable devices are test vectors brought to external pins used solely for test. Unless these pins are properly terminated they can act as unintentional radiators; however, connecting terminating resistors could significantly affect internal propagation delays. It would be recommended that designers only connect these vectors during evaluation and have the vector pin removed or internally unconnected in the production units.

Clock signals should only be admitted via a single pin unless there are two separate clock frequencies. Bringing in the same clock via different traces on the PCB could upset the timing and introduce clock beat frequency noise to the signals and supply lines.

4.3.6 Memory

Other than minimising the speed of memory (ROM or RAM) used to suit the circuit and siting the memory close to the processor to minimise PCB trace lengths there is little that can be done to improve the EMC performance of memory devices.

Read/write memory (RAM) is possibly one of the most susceptible ICs to the effect of transients corrupting data. Typically, data is stored as a charge on a transistor gate

within the device, hence the possibility of a data, address or power line transient causing a corrupted data cell can be quite high. Dynamic RAM (DRAM) is slightly more susceptible than static (SRAM) as the cells are rewritten regularly helping to maintain the charge, but this allows potential corruption via the supply lines during the refresh multiple access to each cell. The difference in EMC susceptibility of DRAM and SRAM is very marginal and both will benefit from transient protection devices on data and power lines, especially if connected to bussed data and address lines without buffered access ICs.

4.4 Analogue Devices

Analogue circuits in general do not have the fast, square waveforms that a digital circuit inherits from its clock, consequently analogue circuits are often not as much of an EMI threat with regards to emissions as digital circuits can be. On the other hand analogue circuitry by definition is capable of reacting to small changes in signal levels and is therefore potentially more susceptible to EMI.

Keeping circuitry to within a specified bandwidth is usually easier with analogue circuits than digital, as rise times (or slew rates) are usually quoted as a maximum value rather than minimum, hence for EMC you should know the worse case condition for the component. If the worse case conditions for emissions are known they can be designed around. Similarly, the circuit itself will often have a maximum bandwidth of response defined by its functional description and adding simple low-pass passive filters operating outside this bandwidth will work without impairing functionality.

The threat from radiated EMI mainly occurs from the potential for demodulation of RF signals within the analogue circuitry and then amplification and/or transmission of a noise signal which, when demodulated, is within the normal operating frequency of the circuit. There are ways this can be limited by design and being aware of the way some components can respond to EMI.

Some analogue circuits are very susceptible to power supply variations, particularly precision amplifiers, audio circuits and ADC. Variations in supply rails can be superimposed on the signal, hence good decoupling and adequate supply line filtering is even more important for some analogue circuits than digital. Mixed analogue and digital circuits need good electrical and if possible physical separation to primarily prevent the digital circuit noise interfering with the analogue functions. Separate supply and ground rails would be recommended, to be connected only where either data is transferred or where the PSU supply enters the PCB.

4.4.1 Amplifiers

The amplifier is one of the basic building blocks of all analogue circuit functions, most other ICs discussed later will have an amplifier circuit of some type within their

circuitry. The design of amplifier ICs can lead to the potential for a highly susceptible device, features which are good on the amplifier specification but bad for overall EMC performance include wide bandwidth, high slew rate, high input impedance and high gain. Amplifiers often feature a high sensitivity to power supply noise as the device amplification is ultimately limited by the power supply rails, also internal current sources can be affected by PSU noise, creating voltage offset errors.

Although losing popularity in many applications, dual supply rail amplifier ICs feature a higher common mode rejection ratio (CMRR) than single rail devices, providing a higher immunity to PSU noise and noise common to both amplifier inputs. Higher voltage supply devices tend to have a higher noise immunity for similar values of voltage gain and bandwidth.

The bandwidth of an amplifier is usually quoted at unity gain (i.e. as a 1:1 buffer rather than actually amplifying). When the bandwidth is reduced immediately gain is produced, hence within functional limits, increasing the gain of each amplifier circuit reduces is effective bandwidth. There is a counter argument to this however, as multiple stages of lower gain, but equal bandwidth, increases the gain fall-off characteristic by approximately 20 dB/decade per stage (e.g. a three-stage amplifier circuit can produce a roll-off of 60 dB/decade). A high rate of gain roll-off reduces harmonic content significantly without affecting the overall circuit signal gain. If a

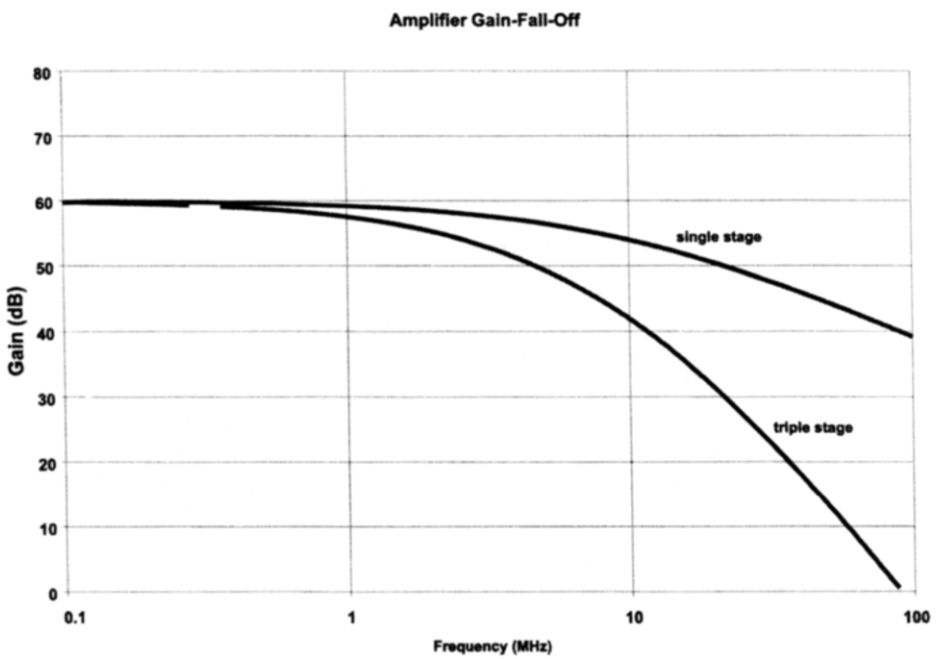


Figure 4.11
Gain roll-off of multiple stage amplifier

signal with a known high harmonic content (i.e. square or rectangular waveforms) is to be amplified multiple gain stages are better than a single amplifier.

The unity gain amplifier configuration can be used in applications where the source impedance of the signal, or signals, varies with frequency. A unity gain amplifier offers a very high impedance to the source, across a wide frequency range (wide bandwidth) and a low output impedance to the next stage of circuitry. Filtering a signal at a unity gain buffer amplifier can prevent noise from entering the target circuit at a very low cost. The signal response can still cover a wide band of frequencies without loss of signal.

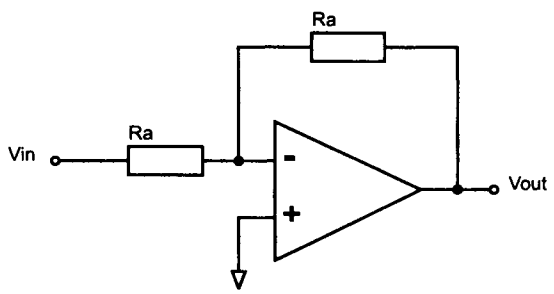


Figure 4.12
Unity gain amplifier

Guaranteed slew rate can be a useful feature, even if higher than required, as at least this allows a fixed filter to be used before or after the amplifier. Slew rate can easily be limited externally on an amplifier using a passive input filter or even in the feedback loop. Filtering in the feedback loop can be useful to change the gain-bandwidth product with frequency by changing the impedance of the feedback element (effectively increasing the roll-off within a single gain stage). If using feedback filtering care should be exercised on the possibility of resonance at higher frequencies causing a bypass of the amplifier itself, also any input noise still impacts the amplifier. Hence if filtering is to be applied it is always best applied to the input stage rather than the feedback circuit.

Current feedback amplifiers can provide a higher immunity than voltage feedback where these are available for the circuit function. Current feedback amplifiers feature a low input impedance, hence are less susceptible to input voltage noise than voltage feedback amplifiers. Another benefit is that the noise gain of the amplifier with current feedback is dependent solely on the feedback resistance (impedance), resulting in an improved noise to signal gain by choice of input resistance.

The main threat to radiated susceptibility in amplifiers, as in most ICs, is from demodulation of RF. In amplifier ICs the results can be more noticeable than in many other ICs as the demodulated signal can be amplified within the device after

demodulation. This is a particular problem where dual supply rail amplifiers have a distinct advantage over single rail devices. In dual rail amplifiers the circuit forms a mirror between the rails and the RF signal should be demodulated in both sides of the circuit, hence appear as a common mode signal. Common mode rejection is high in dual rail devices and the demodulated residual signal is small and centred around the ground point, and therefore should appear as a very small noise signal compared with the input signal. This argument assumes the demodulated signal is within the bandwidth of the circuit function, where it is outside of the bandwidth filtering and control of the gain-bandwidth product should minimise out of band signal interference from any source.

Care needs to be exercised when using a standard amplifier which may be available from different manufacturers (e.g. the 741 operational amplifier). Different suppliers use different designs for the same function, consequently the EMC performance can vary between devices with the same functional specification. If possible and a range of suppliers are to be used, a sample from all the suppliers should be tried and tested against the EMC specification. The internal structure of an IC is going to affect its radiated EMC performance more than its conducted performance given equal CMRR, gain and other functional parametric performance, hence the need for testing in circuit.

4.4.2 Comparators

Comparators are generally insensitive to EMI as the function of a comparator is virtually digital. The output of the comparator is at the positive supply rail if the

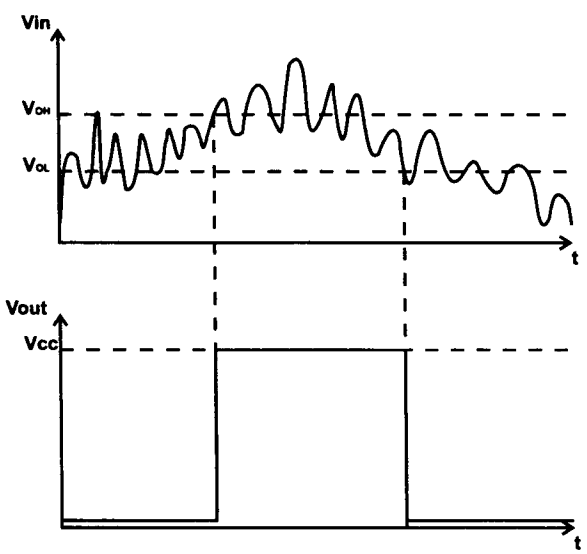


Figure 4.13
Schmitt triggered comparator

positive signal voltage exceeds the negative input voltage, otherwise the output swings to the negative rail. The output can reflect power supply noise, but this is unlikely to affect the device function significantly.

The main threat to circuit stability from EMI occurs at the threshold condition, when the inputs are close. If the input values are close and a noise signal is superimposed on one of the inputs the output can amplify this up to the power supply rail levels, producing a very high-power noise spectrum. A Schmitt-triggered device, which features a voltage hysteresis between the transition states improves immunity, this is directly analogous to the noise margin in digital logic ICs. Consequently, the greater the hysteresis voltage, the greater the immunity level.

4.4.3 Bandgap References

Bandgap references are inherently stable devices as they essentially consist of a forward conducting diode or p–n junction reference, some DC gain stage and biasing circuits (thermal compensation etc.). Consequently, after the supply has been applied the devices are stable and relatively noise free.

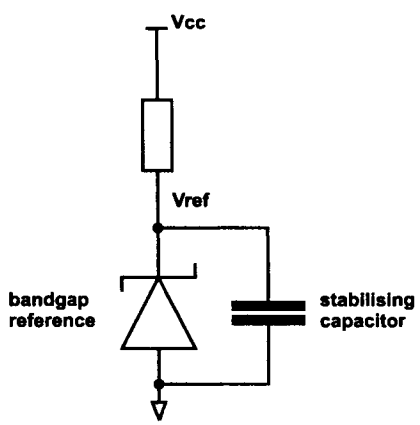


Figure 4.14
Stabilised bandgap reference

The main potential threat to the bandgap reference function is power supply transients. Some capacitance may be required at the device to provide additional decoupling and improve the device's response to transients' demands on the supply. It is unusual to require full ESD protection on these devices and decoupling of a few nF is usually adequate unless the device is in a particularly noisy environment.

4.4.4 Voltage Regulators

Voltage regulators are constructed from a bandgap reference, amplifier/comparator and power pass transistor in their simplest form. It would be expected that the device would therefore be relatively insensitive to EMC issues; however, situations do occur where the linear voltage regulator can create a high frequency internal oscillation. This is primarily due to high open loop gain of the comparator and pass transistor and potential for positive feedback at RF frequencies due to phase shift.

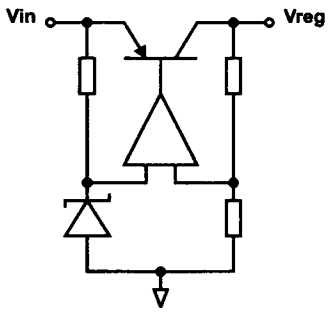
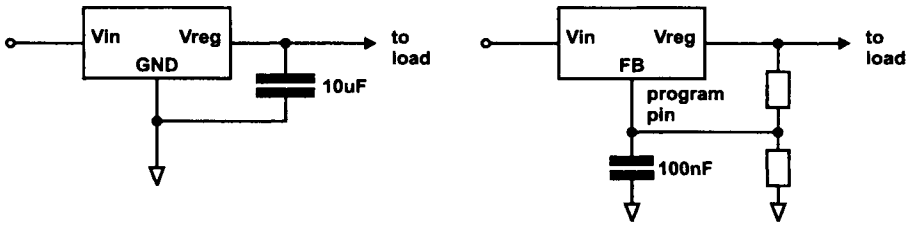


Figure 4.15
Basic voltage regulator circuit

The oscillation problem usually occurs with inadequate decoupling close to the regulator pins. The problem is particularly noticeable if the load is some distance from the regulator, hence there is an inductive lead between the regulated output and load. The output voltage from the regulator leads the load demand, and unless stabilised with quite large capacitance (10 μF/A) the internal comparator oscillates on and off at relatively high frequencies (20 MHz oscillations have been observed on a 5 V regulator supplying only 200 mA in a TO92 package).

Not all regulators suffer this as much as others; however, there is no obvious way to determine this from the individual device specification. Generally, higher current devices are slower to react and consequently do not suffer such high oscillations, having sufficient internal junction capacitances to stabilise the circuit. Devices using Schmitt trigger comparators are also less prone to a high frequency oscillation.

Programmable regulators (i.e. those with a separate voltage feedback pin) are usually easier to stabilise and require smaller capacitors. The stabilisation is added to the feedback/programming pin, and therefore usually a 10 nF ceramic capacitor can be adequate as the current load for the feedback pin is small. It is also possible to sense the voltage at the load and feed this back to the regulator, hence the lead inductance problem is moved from a high current lead to a low current lead reducing the noise problem.



a) stabilising capacitor when load is at a distance from the regulator

b) stabilising capacitor at feedback on programmable voltage regulator

Figure 4.16
Stabilised linear regulator

The most recent developments in linear regulators are for lower voltage drop versions of the standard three terminal devices, termed 'low drop-out' regulators (LDO). These are generally no better or worse from an EMC standpoint to their higher drop-out parents. However, operating at a lower input-to-output differential can reduce the feedback loop instabilities, hence potential oscillation may be easier to prevent with a smaller capacitor.

As with other IC commodity components, regulators are common devices available from many suppliers. Some suppliers exhibit the oscillation problem quite readily whereas others have never experienced the problem.

4.4.5 Serial Interface Devices

Although most often used for communication between digital systems, interface standards such as RS232 and EIA-485 are considered analogue circuits. Unlike many analogue devices they are relatively insensitive to power supply noise due to the digital nature of their signalling schemes. However, as interfaces to external systems they are potentially a source for noise entering the system, and therefore may need higher level of protection than is apparent from their parametric performance specification.

There are many standards for serial interfacing but these can be classified into two groups: single ended and differential. In single-ended systems the signal return is via the circuit ground or reference rail, in differential signalling a separate return signal, or complementary signal line is employed separately from the circuit ground reference. Consequently, with regards to EMC, the differential signalling scheme has advantages over the single-ended scheme; however, differential schemes are more expensive to implement, primarily due to the additional cabling requirements. Table 4.3 lists four of the most popular serial interface standards and their characteristics.

Table 4.3 *Serial interface standards*

Parameter		RS-232-C	RS-423-A	RS-422-A	EIA-485	Units
Mode of operation		single ended	single ended	differential	differential	
Number of drivers and receivers		1 driver 1 receiver	1 driver 10 receivers	1 driver 0 receivers	32 drivers 32 receivers	
Maximum cable length		15	1200	1200	1200	metres
Maximum data rate		20k	100k	10M	10M	bits/s
Maximum common mode voltage		±25	±6.0	–0.25 to 6.0	–7.0 to 12.0	V
Driver signal level	Minimum	±5.0	±3.6	±2.0	±1.5	V
	Maximum	±15.0	±6.0	±5.0	±5.0	
Load resistance (capacitance)		3.0k to 7.0k (2500)	450	100	54	Ω (pF)
Driver slew rate		30	*	**	**	V/μs
Driver resistance		300 (power on)	—	—	—	Ω
High impedance state		300Ω (power off)	±100 (V_o = ±6.0 V)	±100 (–0.25 V ≤ V_{cm} ≤ 7 V)	±100 (–7 V ≤ V_{cm} ≤ 12 V)	μA
Minimum receiver resistance		3.0	4.0	4.0	12.0	kΩ
Receiver sensitivity		±3.0	±0.2	±0.2	±0.2	V

*Determined by cable length and data rate.

**Determined by IC used.

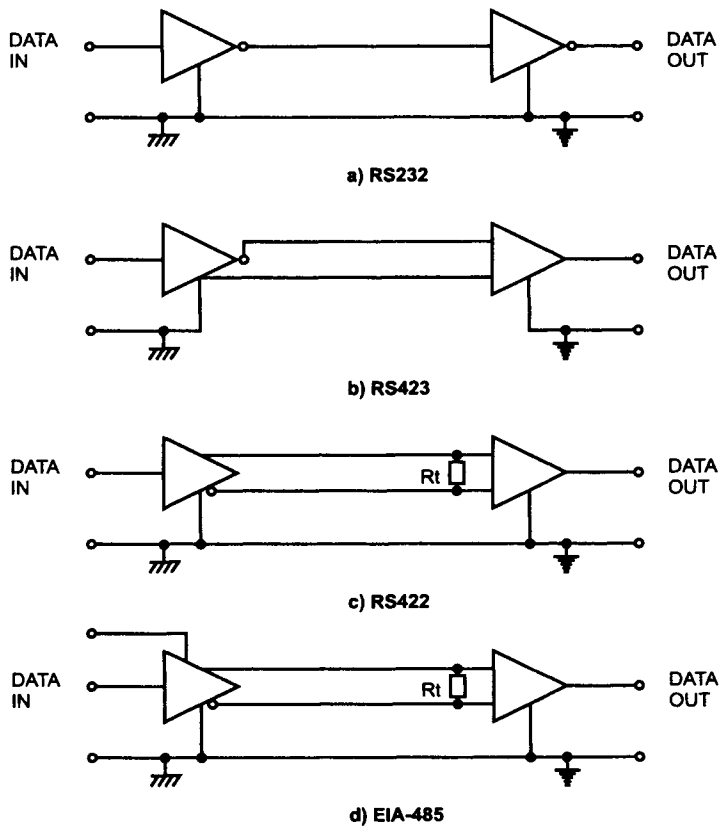
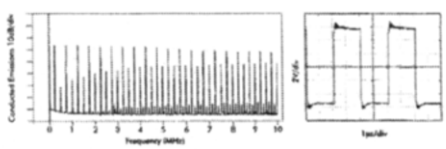


Figure 4.17
Interface standards wiring schemes

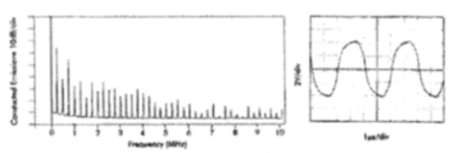
Single-ended schemes are similar in principle to most digital logic signalling schemes, except that higher voltage levels are used and signalling is usually between a positive and negative voltage (e.g. with typical RS232 circuits signal levels are between +12 V for logic '1' and –12 V for logic '0'). Single-ended serial interfaces have a much higher immunity to interference than logic circuits due to these higher signal voltage levels; however, as the cables are in external uncontrolled environments they can be expected to see higher levels of noise than circuits boards within a system. Single-ended schemes are rarely terminated resistively, hence sit in a high impedance state and rely on the high voltage level of the signals as a barrier against false triggering. The problem of high impedance on single-ended lines is that interference can produce a voltage offset on the ground line, even the signalling itself can create ground bounce offset, hence reducing the noise immunity of the signal line. The ground levels of two interconnected systems can also be offset by a significant DC level due to independent reference points or even feedback ground current, which again reduces the signal switching level in absolute terms and therefore reduces the noise immunity.

Differential schemes offer high levels of immunity with lower signal levels as these operate on the difference between two signal levels and not an absolute voltage level. Having differential signals also increases the level of common mode rejection from the signalling system as interference on the cable superimposes on both signal carrying lines and sums to zero at the receiver circuit. The most popular differential schemes (RS-422 and EIA-485) also require resistive termination of the data line for correct operation. As well as resistive termination reducing reflection and ringing, resistive termination also reduces the potential for cross-talk and interference as the lines are linked by a low-impedance connection and can sink noise voltage or current induced in the cables.

Emissions from serial interfaces can be reduced by the use of slew rate limited signalling devices. These devices operate using a controlled rate of switching, producing slower edges on signals and, consequently, lower harmonic content in their spectra. For example, an EIA-485 interface operating at 250 kHz signal rate using an interface IC without slew rate limiting can exhibit significant noise spectra above 10 MHz without significant fall-off of power density. Using a slew rate limited device for the same signal and the harmonics are almost extinct by 5 MHz (Figure 4.18).



a) standard 485 interface noise spectra with 250kHz signal rate



b) slew rate limited 485 interface noise spectra with 250kHz signal rate

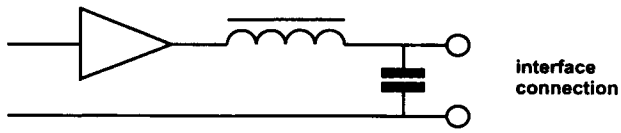
Figure 4.18

Noise spectra of standard and slew rate limited EIA-485 interfaces

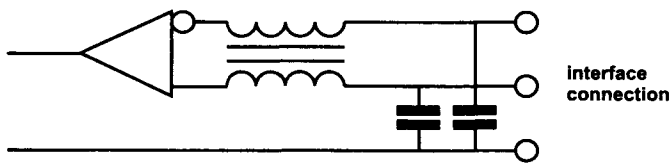
Slew rate limited ICs are available to drive most interface standards and RS232 has a slew rate limit in its specification (see Table 4.3). Slew rate limited ICs are often restricted on the maximum transmission frequency at which the interface can transmit data (slew rate limiting only affects transmission rates). In the majority of cases this should not be a problem as the rates are still high, but in speed critical interfaces slew rate limited switching may not be suitable.

Filtering can be used for both immunity and emissions reduction. Basic passive filters are adequate to produce some slew rate limiting on the transmission and filter

noise at the receiver. A common mode choke arrangement is typically used on differential signal lines with a simple differential filter for single-ended schemes (see section on inductors for calculation of component values).



a) single ended scheme passive filter



b) differential scheme passive filter

Figure 4.19
Filtering serial interface lines

Another technique commonly used to improve the EMC performance of an interface circuit is to isolate the interface. There are several off-the-shelf isolated interface hybrid devices available which in many cases provide single chip solutions to the interface isolation circuit. Alternatively, the interface can be isolated using discrete components, using opto-isolators for the data and either a DC–DC converter or transformer and switching power supply device for the supply line. Having an isolated interface significantly increases the noise immunity as even ground-induced noise becomes common mode at the interface, also ground offsets between systems are reduced as the interfaces are no longer referenced to the system ground.

As an accessible port in a system, ESD is also a significant potential threat to an interface circuit. It is also a likely access point of ESD to other in-board circuits, hence the interface is the best location to provide ESD protection. Single-ended systems are usually easiest to protect using a single bi-directional transient voltage suppressor device. With differential signalling several devices may be required on either line and the loading capacitance will have to be minimised for the higher speed signalling lines. Some of the best methods are to include the ESD protection components within the connector (see section on connectors). Many IC manufacturers recognise the threat of ESD on interface circuits and integrate protection into the interface IC itself; however, the ESD pulse could still create

interference on other in-board circuits and discrete protection at the connector terminals provides a degree of protection for the entire system, not only the interface IC.

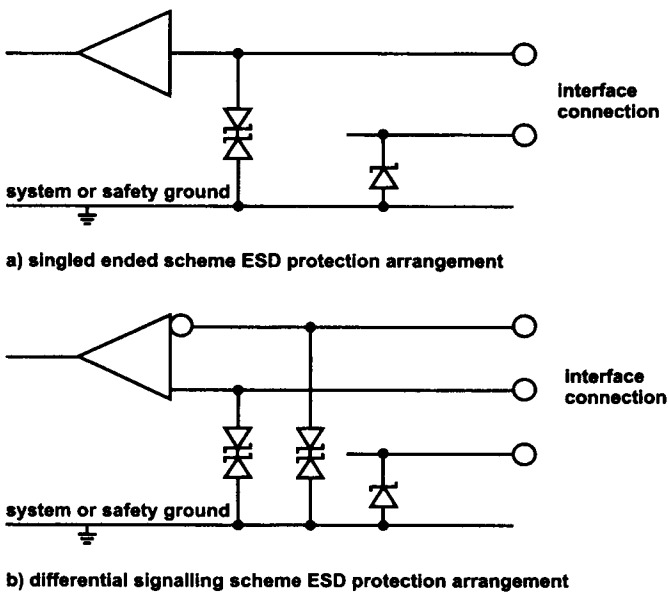


Figure 4.20
ESD protection devices at interface connection

4.4.6 Data Converters

Analogue-to-digital (ADC) and digital-to-analogue (DAC) converters are often an interface between an enclosed digital system (e.g. microcontroller) and an external analogue process (e.g. measurement of some physical parameter such as temperature). Consequently, as with serial interfaces, there is a potential for both susceptibility and emissions via the converter circuits.

There are additional reasons for considering the noise content of the analogue signal due to potential false data values being generated by the converter. The ground rail and supply lines for the analogue and digital sides are also usually separated and only connected either at the IC pins or even on-chip in some instances.

The level of noise that can create a problem is the analogue voltage resolution (V_{AR}) and is relatively easy to calculate for ADC/DACs. It is related to the digital resolution (i.e. number of bits, n) and the full scale analogue voltage swing (V_{FS}).

$$V_{AR} = \frac{V_{FS}}{2_n} \quad 4.2$$

Therefore, for an eight-bit device with a 0–5 V full-scale range, the analogue resolution is 19.5 mV and noise above this level could produce false data. A 16-bit device with the same analogue full-scale range is sensitive to only 76 μV of noise. Hence higher bit converters will be more sensitive to noise than lower bit devices, or alternatively the analogue range could be increased to compensate for each additional bit.

The speed of ADC/DAC converters is usually much lower than the digital processing circuit and filtering of the analogue signal is easily implemented with passive components. Alternatively, some analogue signal processing (e.g. sample and hold, amplification) can be applied directly to the analogue signal and include the filtering in the active circuit.

The signal can even be digitally filtered, for example the digital value can be repeatedly read from the ADC (or written to the DAC) and the numerical average taken, or more complex error correction algorithms can be applied. The digital filtering techniques can only be applied when the analogue sampling rate is lower than the digital sampling rate (i.e. the analogue signal rate of change, or slew rate, is slower than the digital sampling frequency). Digital sampling of this type can be achieved with additional software rather than electrical components, so the filtering cost can be written off in the development stage and, providing the additional code fits in available memory, there is no component count increase.

One common feature to almost all types of mixed signal converter that significantly affects the EMC is the stability of the voltage reference device used within the circuit. The reference is frequently on-chip, but available to an external pin for decoupling. A relatively low value of capacitance is required, typically 10–47 nF being adequate, but if available the manufacturers' guidelines should be followed. The reference is used to determine the analogue signal value by comparison via other on-chip circuitry (parallel resistor ladder, successive approximation or dual slope) and often has a low value; therefore, with a high-bit converter the level on analogue noise on the reference required to cause false data is very small (tens of microvolts typically). If an external voltage reference is used the notes above for stabilisation should be followed and the device should be sited close to the converter and over the same analogue ground plane.

The type of converter used is usually dictated by application so the EMC performance is secondary; however, as with most devices the slower the device operation the lower the potential for EMI problems. With signal converters the fastest types are usually parallel or flash converters, these present a relatively large instantaneous load on the supply on the conversion clock edge. Flash converters should only be used where their speed is essential (e.g. video digitising circuits and digital storage oscilloscopes or DSOs).

Successive approximation converters are used for medium speed conversion, typically up to a few million samples per second (MS/s) in processing and instrumentation applications. This type of converter offers a reasonably even load

demand on the supply as the on-chip conversion progresses in single steps. Consequently, the noise generation on the supply line is relatively low. Dual slope types are typically the slowest and the lowest supply noise generators.

The synchronisation of signal converters and control logic is usually not necessary for correct operation. The controller reading the converter is often operated at a much higher rate than the analogue conversion process so that data can be read or written, processed and the result communicated to other devices while the next conversion is being performed. Even high-speed video DACs and DSO ADCs operate on signals in the digital domain at a much higher rate than the analogue signal is sampled. This allows the converter to be deliberately operated either asynchronously or delayed from the digital system clock.

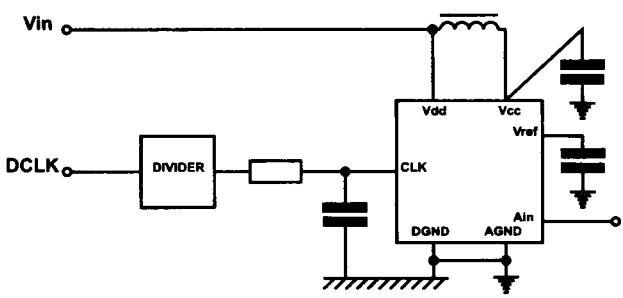


Figure 4.21
RC time delayed clocking

Full asynchronous conversion has little benefits as regards EMC and the asynchronous conversion cycle can create beat frequencies with the digital circuit. However, an offset clock signal has a benefit to the converter as the conversion edges are slightly offset from the digital clock edges, hence the noise from the digital circuit supply occurs at a different instant to the analogue sample. With adequate decoupling on the converter this slight clock offset can significantly reduce the effect of the digital supply noise affecting the analogue signal. The delay can be generated simply using an RC network which will also slew rate limit the conversion clock signal into the converter, again benefiting the EMC performance.

Circuit layout can prove critical to full functional performance of the converter. Similar principles to interface ground separation need to be applied to the analogue and digital supply lines (see Chapter 6). The supply for the analogue and digital circuits should be separated at the device. If the analogue supply is derived from the digital rail it should be filtered using an inductor or ferrite bead and have a separate decoupling capacitor on the analogue supply input pin. The analogue ground should be separated and be used to provide a guard ring and/or surface ground fill for the analogue circuit sections up to the analogue signal connector.

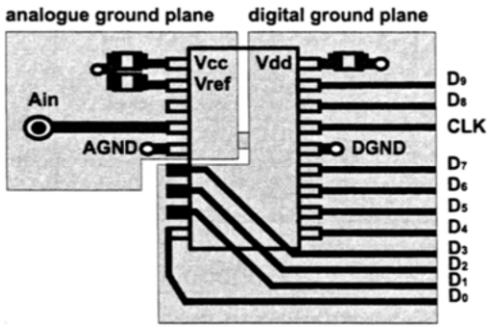


Figure 4.22
PCB layout for ADC/DAC

ESD protection used for serial interfaces can also be applied to a signal converter analogue input/output connection.

4.4.7 Power Supply Components

A modern trend in power supply design, and hence in associated ICs, is to use a switching technique to produce step-up and step-down supply rails at a high efficiency. The linear regulator (see above) is still popular, but these newer switching regulator circuits are becoming more commonplace as an alternative high-efficiency replacement.

The switching regulator is a significantly higher EMC threat than a linear regulator as it has an inherent oscillation, hence noise source, for its functional operation. Coupled to the controller/oscillator IC is usually a magnetic component, either a transformer or and inductor, possibly an external power transistor and several other passive devices to complete the circuit. There are a multitude of potential EMI generators within a switching power supply circuit and whereas most of the other analogue ICs are potential EMC victims, the switching power circuit is a potential EMC aggressor.

There are several choices that can be exercised over the IC as well as the peripheral circuitry. Although a high maximum switching frequency can equate to smaller magnetic and filter capacitors, maintaining a primary switching frequency below 150 kHz can reduce conducted noise significantly within the regulatory band and make filtering easier. There are also choices of switching topology that will affect the noise characteristics of the completed circuit.

The most basic controllers feature a simple fixed frequency switching circuit to drive a magnetic component and the output is determined by the value of the magnetic component (either the value of an inductor or the turns ratio of a transformer). This type of supply is an unregulated circuit and noise content is easy to filter and often low due to the low-power levels these circuits can handle.

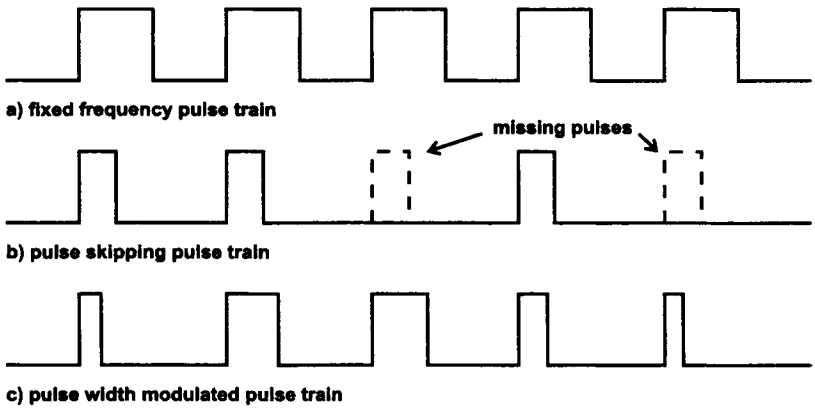


Figure 4.23
Various switching technique typical pulse trains

Pulse skipping controllers work by having a fixed pulse width and frequency and omitting occasional pulses to regulate the output voltage from the circuit. This topology is relatively simple and having a fixed frequency and pulse width gives a great advantage to the noise characteristic, the maximum repetition rate is known and can be filtered and most other noise is a sub-harmonic of this, hence a low EMC threat.

A popular technique for higher-power levels (20–100 W) is pulse width modulation (PWM). The controllers for this switching technique regulate the output voltage by controlling the width of the pulse, usually with a fixed repetition rate (frequency). Another factor which can be controlled or limited is the duty cycle, from 0% to 100% of the repetition rate. Limiting the minimum duty cycle to a known value helps to minimise the high frequency content, as very narrow pulses create high-frequency harmonics. PWM techniques are more EMC aggressive than pulse skipping or fixed frequency techniques due to the uncertain nature of the pulse train and the difficulty in filtering over a wide modulated pulse range.

Soft switching techniques are another method of limiting noise content of switching circuits. Soft switching is not necessarily simply slew rate limiting the pulses, but usually entails allowing the magnetic circuit to saturate and the energy to decay to zero before the next switching cycle is initiated. These types of circuits are also known as resonant mode as they make use of the self-resonance of the magnetic circuits to determine pulse timing. The techniques offer low losses as the switching circuit itself does not have to remove any energy from the magnetic element for the next switching cycle. Figures determined from simple unregulated 50 W switching converters suggest soft switching techniques can reduce conducted noise by as much as 30 dB.

Circuits switching large current loads and power levels exceeding a few hundred watts may use zero crossing controller ICs to achieve low conducted noise. These controllers have a topology which has a state during the cycle in which either no current flows (zero current crossing, ZCS) or no voltage differential is applied to the magnetic element (zero voltage crossing, ZVC). This gives a low conducted noise as the transition of switching occurs during a zero energy state on the magnetic element (the technique is also popular with motor controllers). Zero crossing techniques can be used with other control modes and are particularly useful for high-voltage circuits.

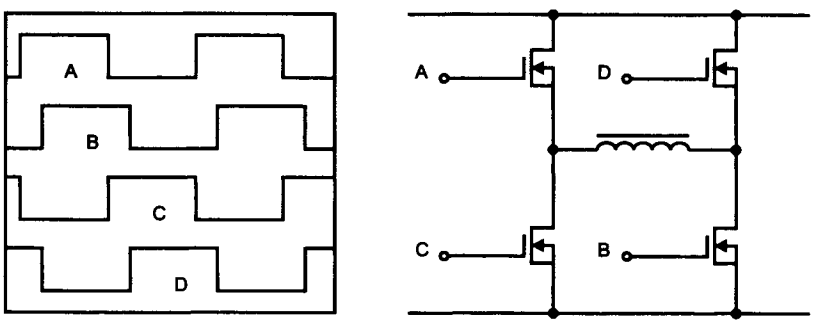


Figure 4.24
Zero crossing H-bridge transformer driver

The main threat for radiated noise in power supply circuits occurs from fast switching edges and the magnetic circuit element (see section on inductors and transformers). Even low frequency switching ICs can produce fast rise times for the drive and these may need limiting externally. PCB layout and grounding schemes will need considerations and ground return loops within the PSU circuitry should be treated as high speed lines and tracked close to the supply feeds for minimum loop area and maximum coupling.

As with linear regulators, the potential for internal resonances can occur in the feedback loops in power supply circuits if the open loop gain of the feedback system is very high. The feedback loop may need its own decoupling and capacitive compensation to reduce its operating speed. The requirement for fast response to transient load demand in modern supply circuits makes the limiting of the feedback circuit response difficult to justify in many instances, particularly for microprocessor circuits. Using simple feedback circuits which have a near digital response (on/off) may be better for fast load demands than a high gain analogue feedback system (e.g. slope compensation).

A recent approach to active noise suppression in power supply circuits is the power supply damping circuit (PSDC). This is essentially an active frequency-dependent shunt resistor which is high impedance at low frequency and low impedance at high

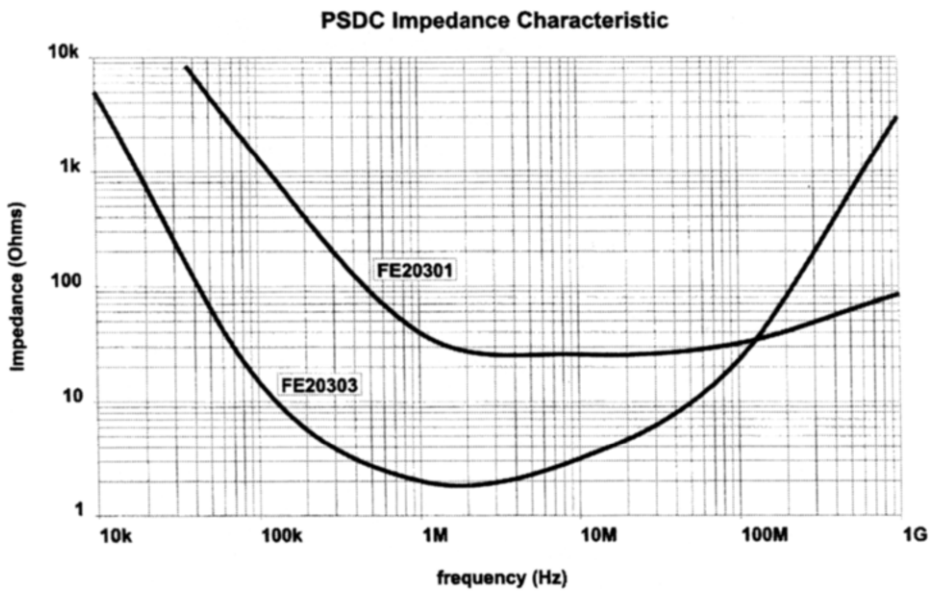


Figure 4.25
PSDC impedance analysis

frequency. Hence noise on the power supply is shunted to ground between certain frequency limits. The device does not offer as low an impedance as some capacitors, but the frequency range over which the low impedance extends would require multiple parallel capacitors to achieve. The range of devices is relatively restricted, primarily aimed at 5 V DC supply rails. The cost is also significantly higher than the cost of a capacitor, but the device does offer a higher level of noise suppression for certain power supply applications.